IC Design Methodology- Be the Lead

To remain competitive in this tight job market, it is essential for all Semiconductor professionals/ IC Design Engineers to “sharpen their skill set".
We recently launched up a startup "Catalyte IC Design"- one of our primary focus is "Trainings on High-end IC design". CatalyteIC will offer a short seminar in Santa Clara, California on July 24 (Fri). Here's the information for the seminar.

What- IC Design Methodology- Be the Lead
When- July 24 (Fri), 12 - 1 pm
Where-
TiE, Silicon Valley Chapter
2903 Bunker Hill Lane, Suite # 108, Santa Clara, CA - 95054

Intended Audience

1. Anyone involved with some phases of IC design (e.g. - Verification, RTL, Synthesis, Physical design, and Layout, Analog and RF design, EDA, PDK) - Expand understanding with **all phases** of the design flow.
2. Anyone involved with semiconductor industry (e.g. - Design, Process, Product and Test Engineering, Library/PDK) - Widen the Horizon

Outline of the Presentation

- Module1- Designing an IC- Concepts through Implementations
- Module2- Custom Design Flow– Default to Power
- Q/A

Presenter

Faizul Alam
Chief Technology Officer
Catalyte IC Design

Additional info-
www.catalyteic.com