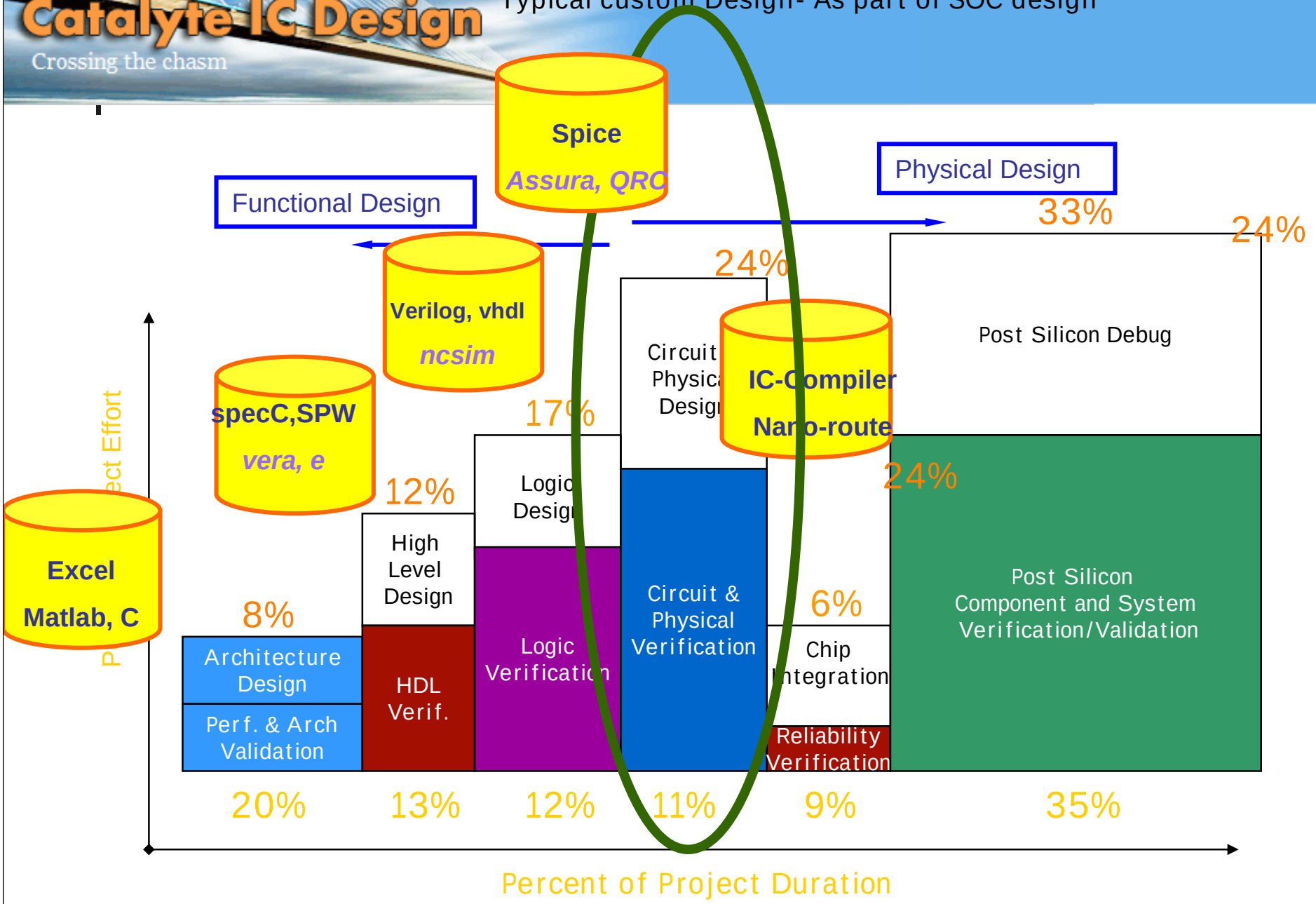
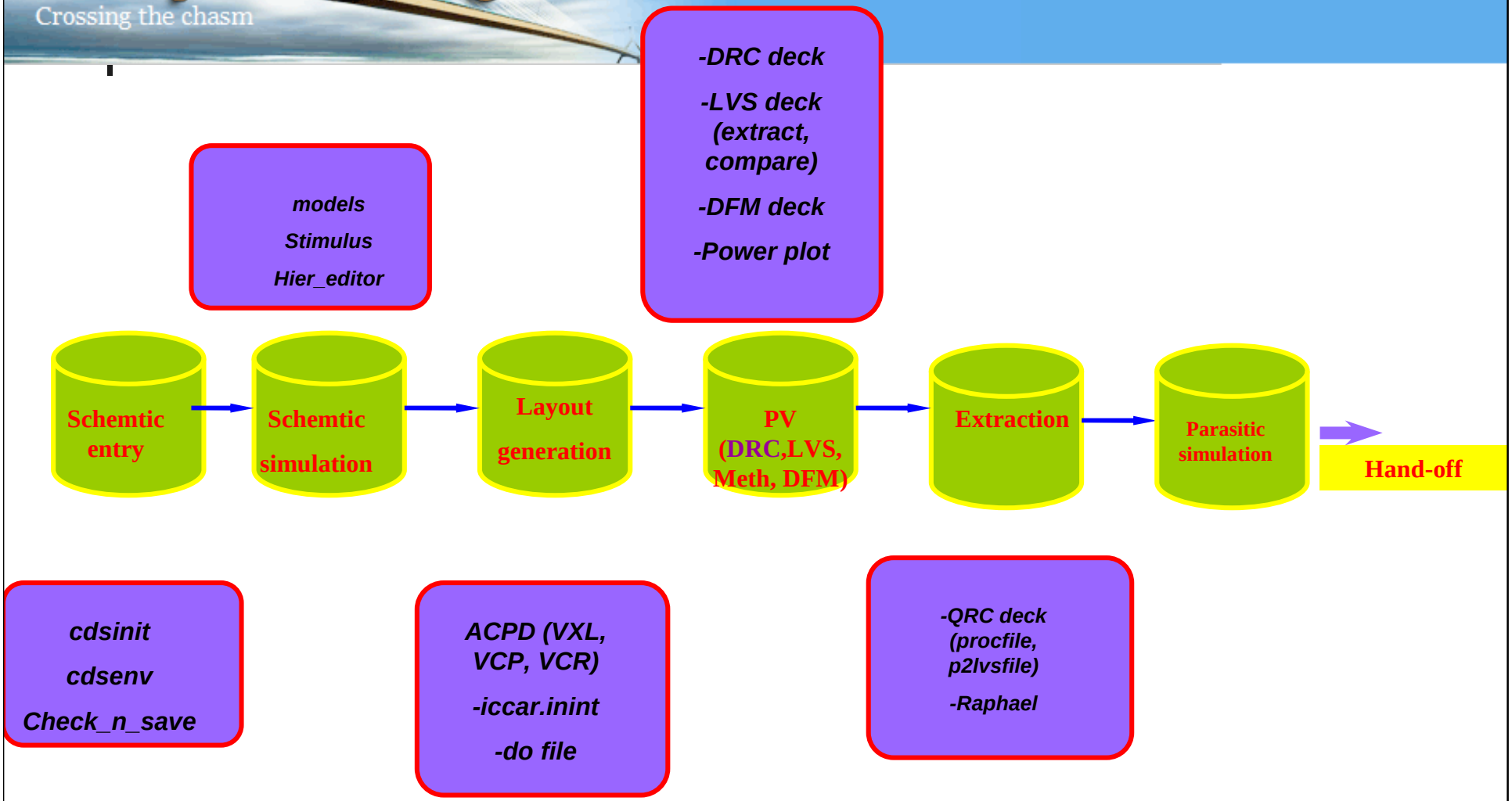
Catalyte IC Design

Crossing the chasm

Typical custom Design- As part of SOC design

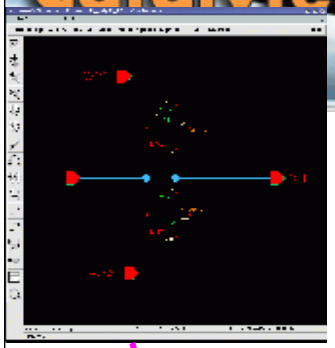


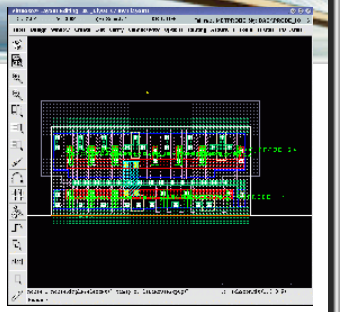
Physical Design Implementation (Control files)

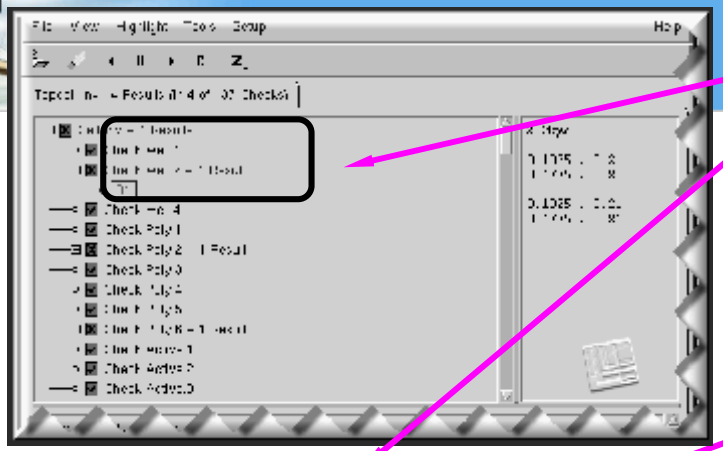


Catalyte IC Design

Circuit and Physical Design Implementation Flow (Phases, Views)

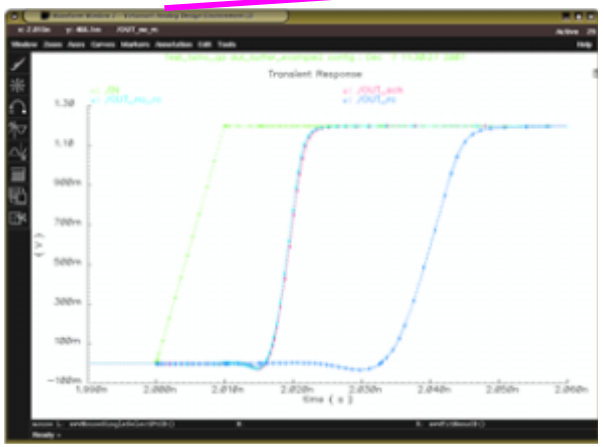




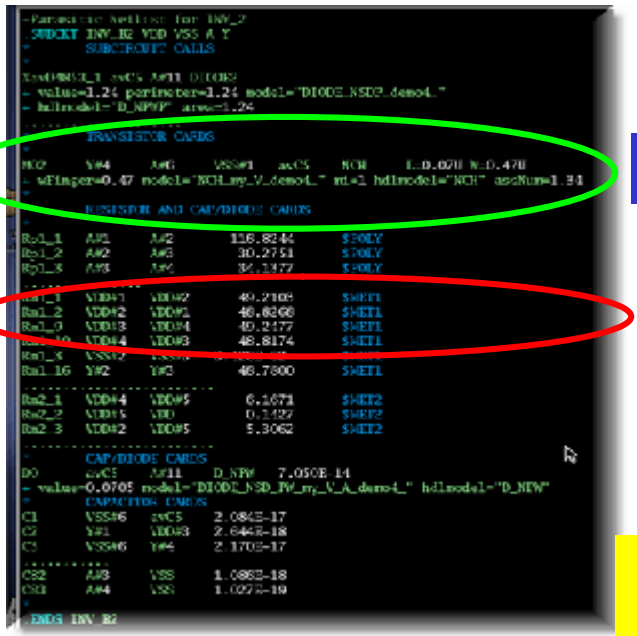


DRC- Nwell spacing violation

Schemtic entry → Schemtic simulation → Layout generation → PV (DRC,LVS, Meth, DFM) → Extraction → Parasitic simulation → Hand-off



Buffer output- schem. Vs parasitic simulation



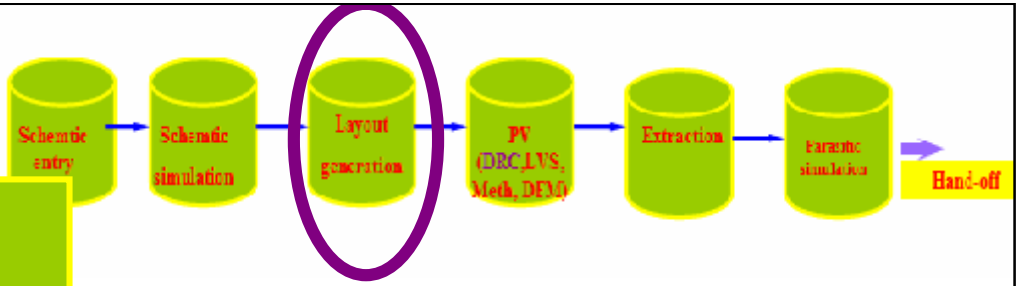
Designed device

Parasitic Res

schem. Vs parasitic netList

Catalyte IC Design

Layout generation

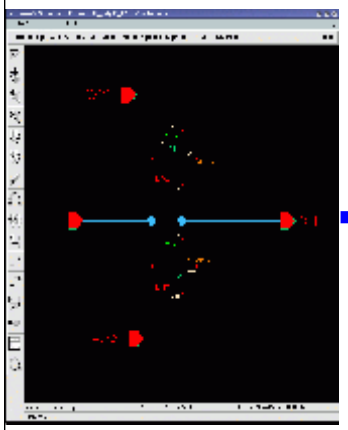


Tool specific

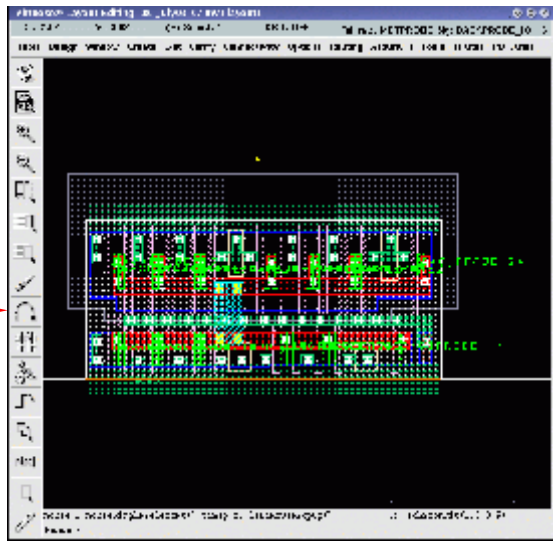
1. Full Custom

2. ACPD (VXL, VCP, VCR)

3. Skill procedure (pinReport, zoom2Point, trimLSW, ..)



Layout generation



PDK input

-Techfile

-display.drf

-pcell

-icc.rul

Major tool-

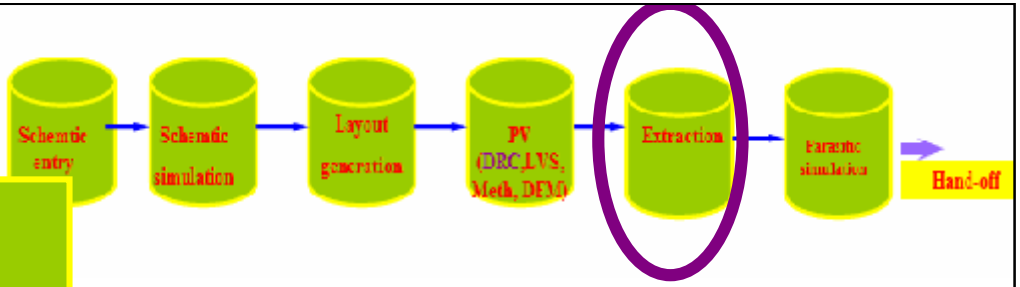
-Virtuoso

-IC Station

Catalyte IC Design

Crossing the chasm

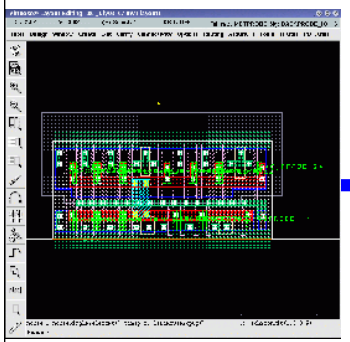
Parasitic Extraction



Tool specific

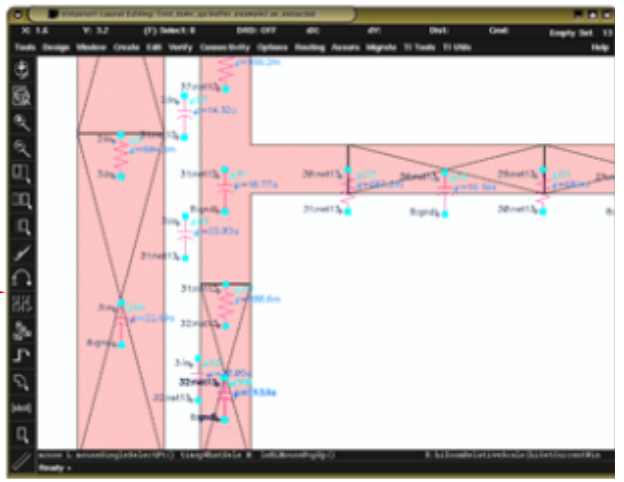
-Performance vs. accuracy

(extType, Filter, outputNetlist)



Parasitic extraction

(R, C, L, K)



PDK input

-procfile (cap)

-p2lvsfile (Res)

Major tool-

-QRC/RCX

-startXT

-calibre xRC