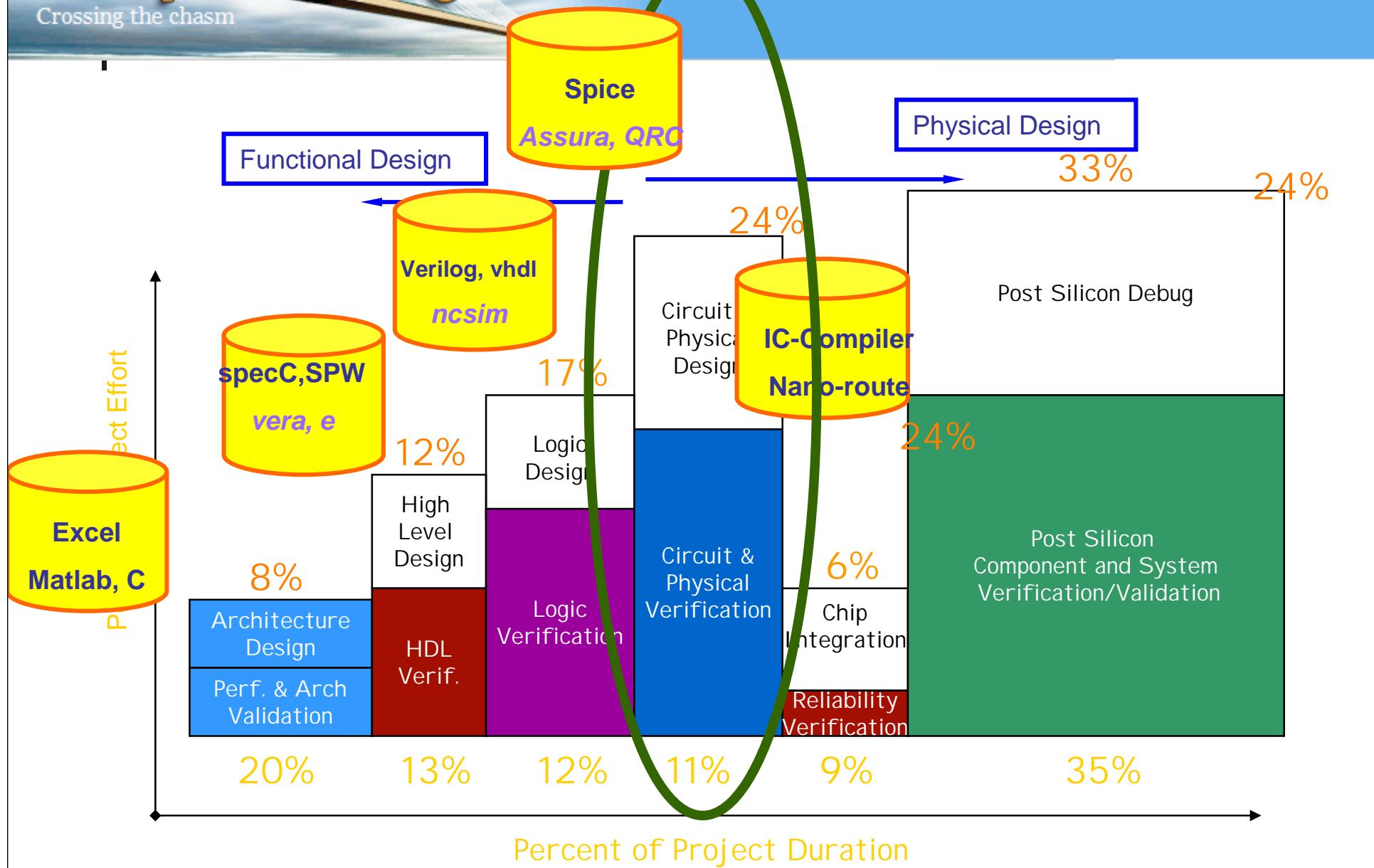
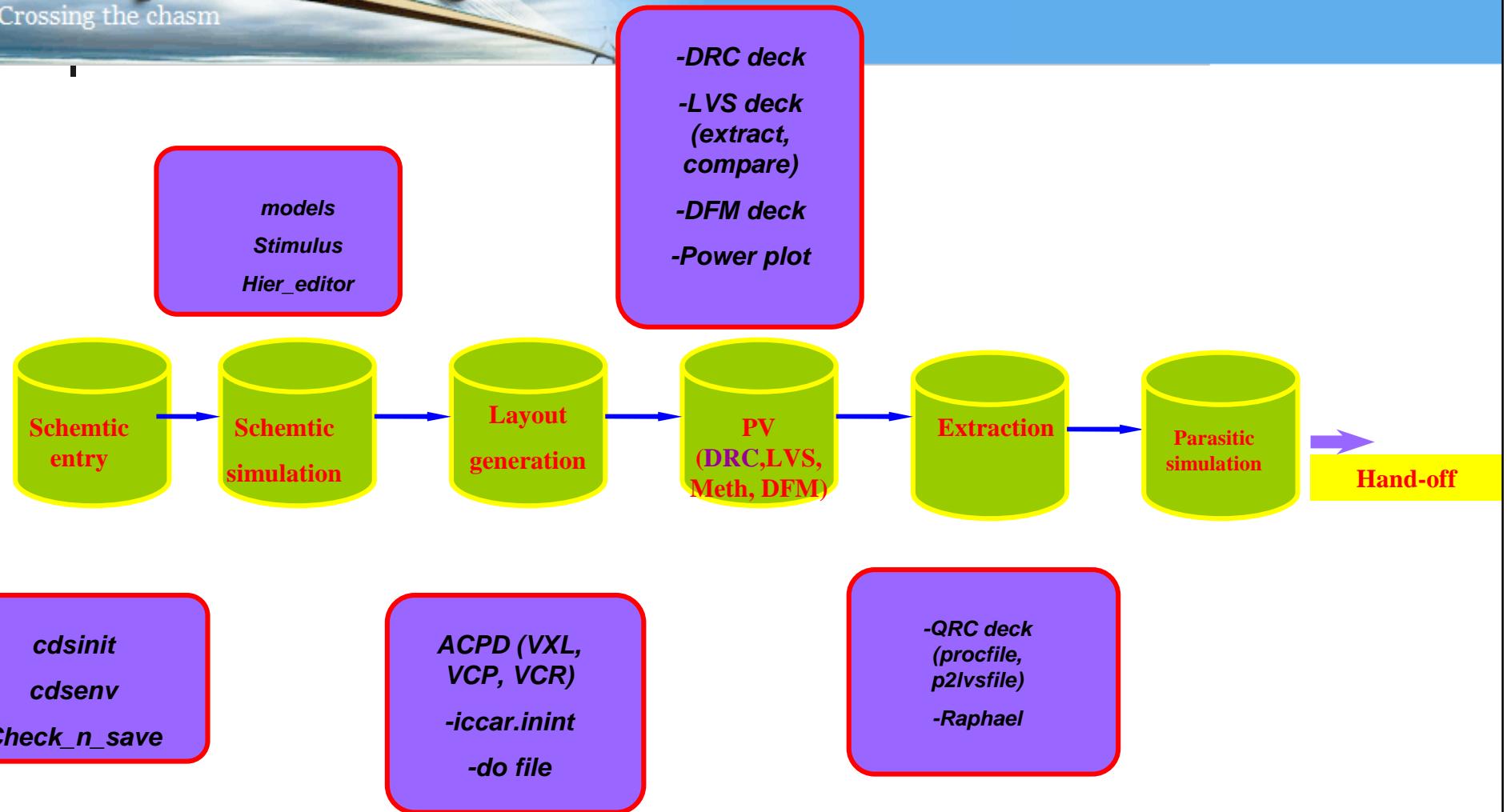


Catalyte IC Design

Crossing the chasm

Typical custom Design- As part of SOC design





Catalyst IC Design

Circuit and Physical Design Implementation Flow (Phases, Views)

Schematic entry

Schematic simulation

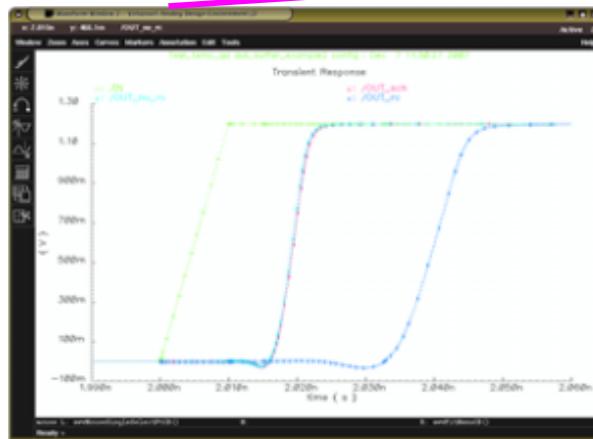
Layout generation

PV
(DRC,LVS,
Meth, DFM)

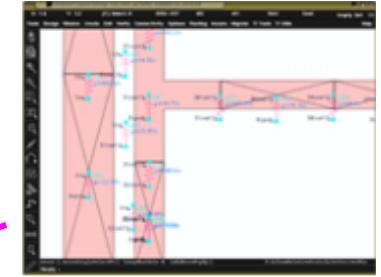
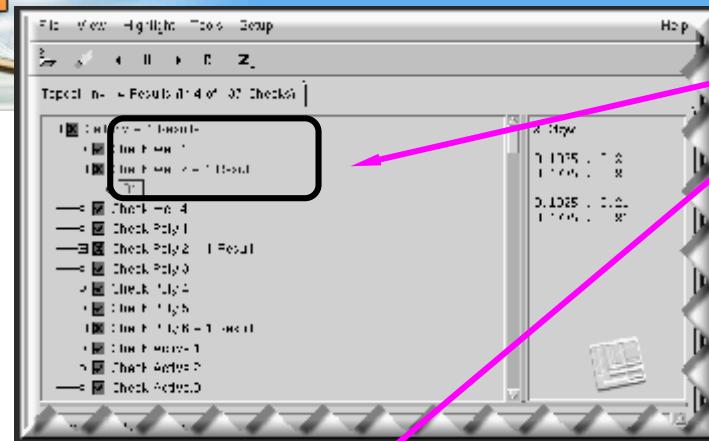
Extraction

Parasitic simulation

Hand-off



Buffer output- schem. Vs
parasitic simulation



```

-- Parasitic netlist for INV_2
-- SICKY INV_2 VDD VSS A Y
-- SUBCIRCUIT CALLS
-- 
-- Transistor CARD
-- 
MOS1_VN4_A00_VSS01_wx05_NOR_E=0.020_W=0.470
- wLinger=0.47 model="MOSINV_V2_demo4" m1=1 hdLmodel="NOR" aschNum=1.34

-- RESISTOR AND CAPACITOR CARDS
-- 
Rn1_1_A02_A02 156.8244 SPOLY
Rn1_2_A02_A02 30.2751 SPOLY
Rn1_3_A02_A02 36.1377 SPOLY

Rn1_4_VN041_VDD42 46.2105 SPWELL
Rn1_5_VDD42_VDD45 46.6266 SPWELL
Rn1_6_VDD43_VDD44 46.2177 SPWELL
Rn1_7_ATDD44_IDDD45 48.8174 SPWELL
Rn1_8_VN042_VDD42 46.7300 SPWELL

Rn2_1_VDD44_VDD45 6.1671 SPWELL
Rn2_2_VDD45_VDD40 0.1429 SPWELL
Rn2_3_VDD42_VDD45 5.3062 SPWELL

-- CAPACITOR CMOS
DO_d05_A01_D_NPW_7.050E-14
- value=0.0705 model="DIODE_NSD_INV_m1_V_A_demo4" hdLmodel="D_NPW"
-- CAPACITOR CMOS
C1_VSS46_ZNC5 2.084E-17
C2_YNL_IDDD45 2.644E-18
C3_VSS46_IDDD45 2.170E-17

-----CS2_A03_VSS 1.086E-18
CS3_A04_VSS 1.027E-19
-----ENDS INV_2

```

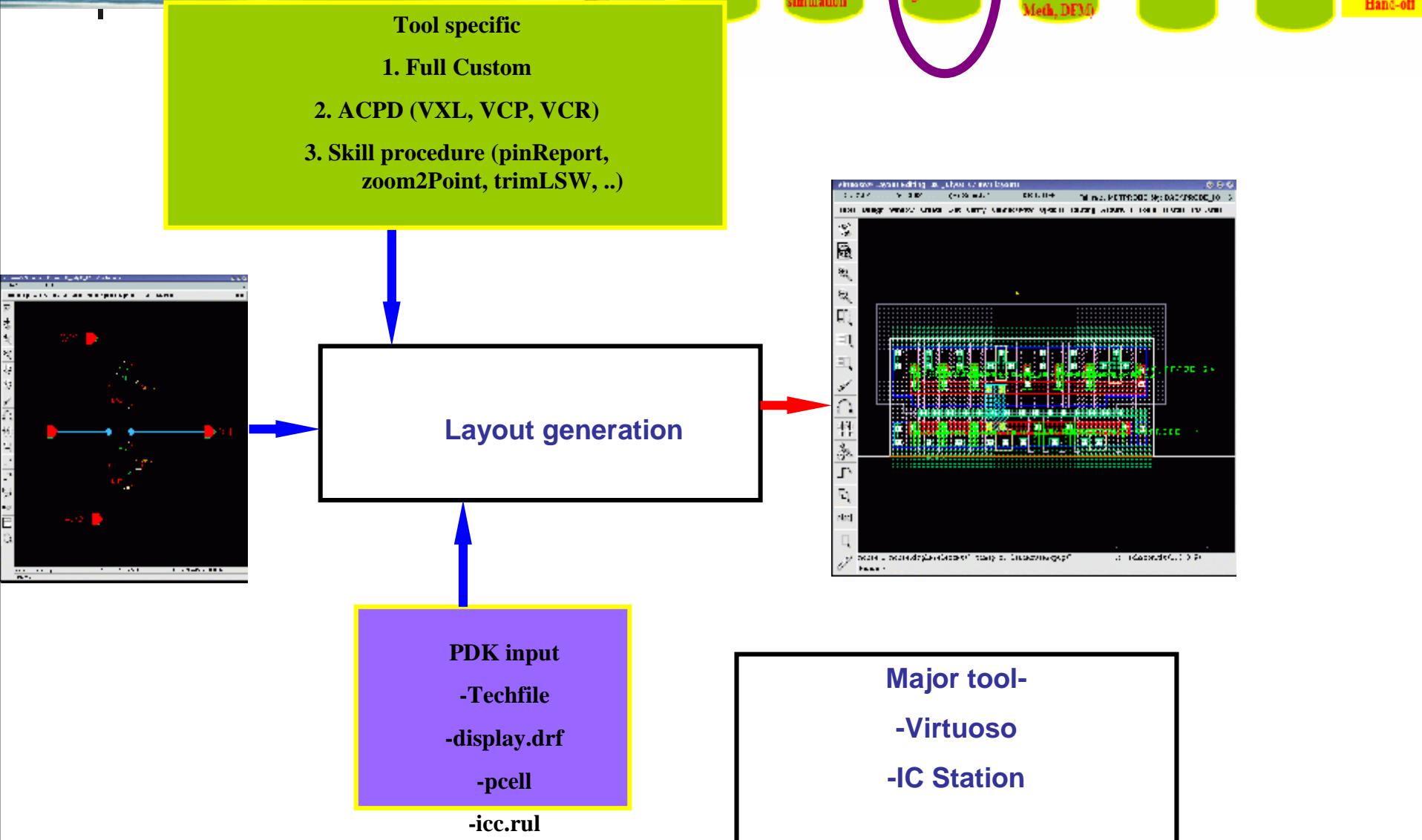
Designed device

Parasitic Res

schem. Vs parasitic
netList

Catalyte IC Design

Layout generation



Catalyte IC Design

Crossing the chasm
Parasitic Extraction

