Fundamentals of Silicon Processing and Microelectronic Devices- An Overview

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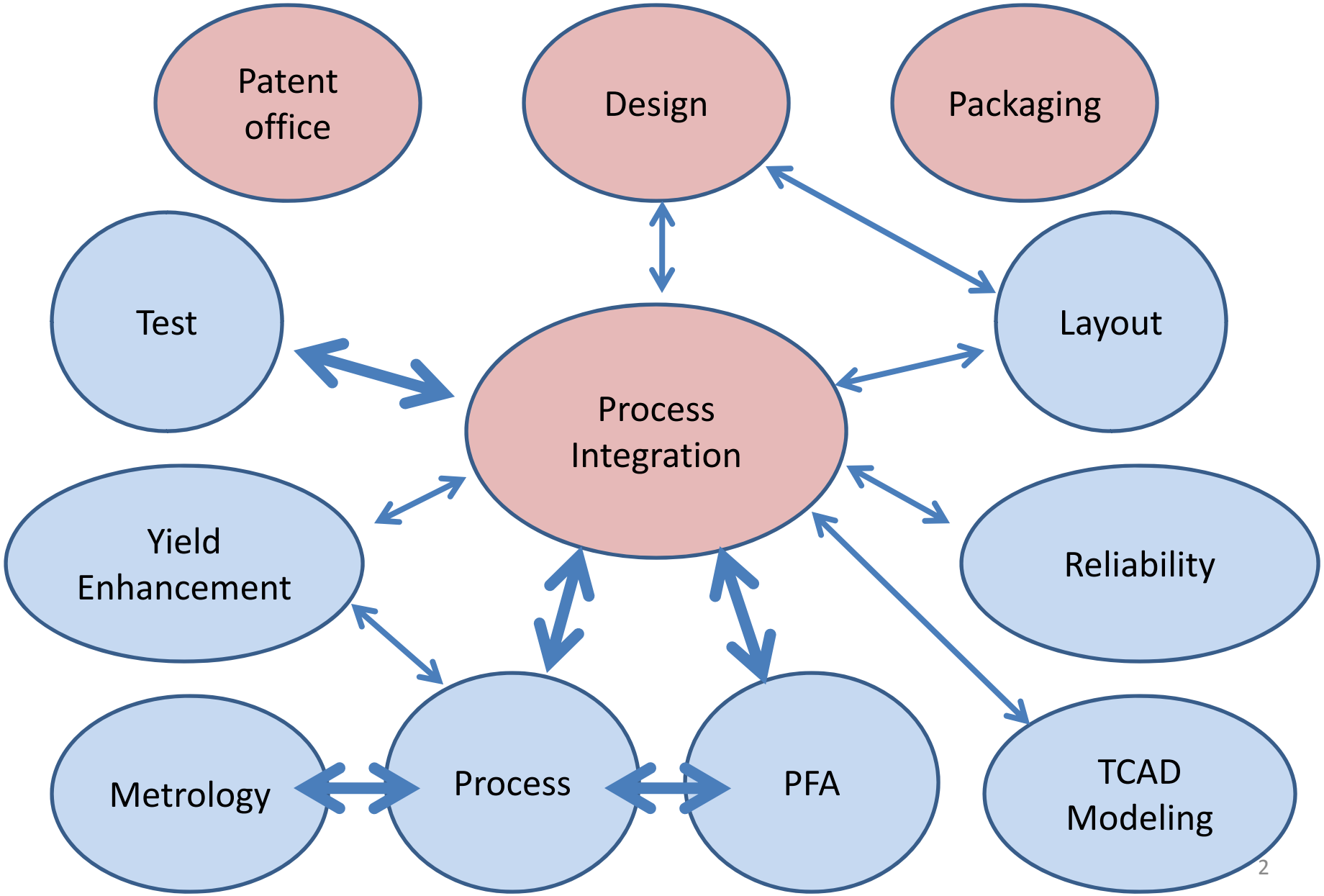
Semiconductor Manufacturing

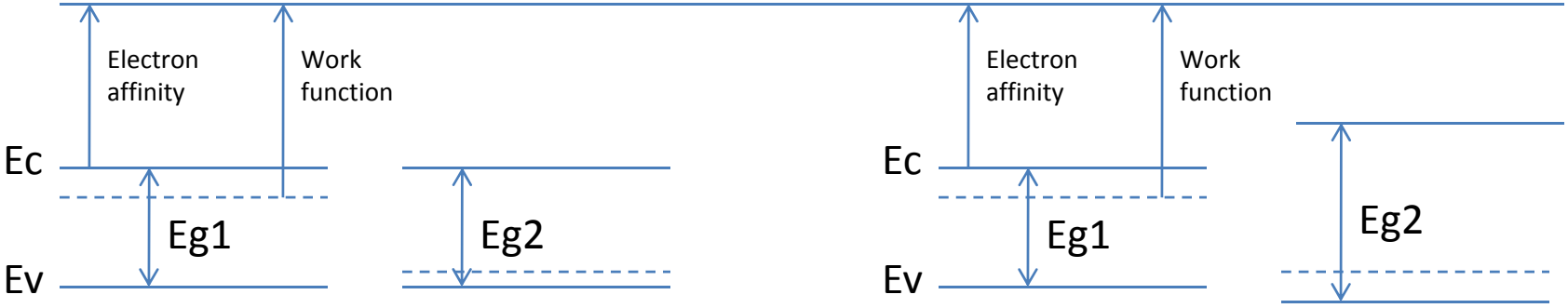


Two groups of Semiconductors

Elemental Semiconductors: They are single elemental Semiconductors, from column IV of the periodic table (Si, Ge, C).

Compound Semiconductors: They are formed by using two or more elements from groups II through VI of the periodic table. For example from group III –V compounds is GaAs, GaP.

Homo-Junctions (Eg1 = Eg2) **Hetero-Junctions (Eg1 ≠ Eg2)**



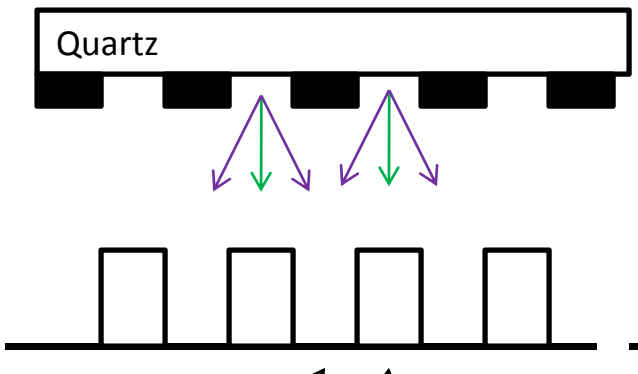
eV (Electron Volt): The kinetic energy gained by an electron if it starts at rest and drops in a potential difference of 1-volt.

Electron affinity: The energy needed to move an electron from the edge of the conduction band (Ec) and place it outside of the material (Vacuum)

Work function: The energy needed to move an electron from the Fermi level (Ef) and place it outside of the material (Vacuum)

Phase shift mask

Binary

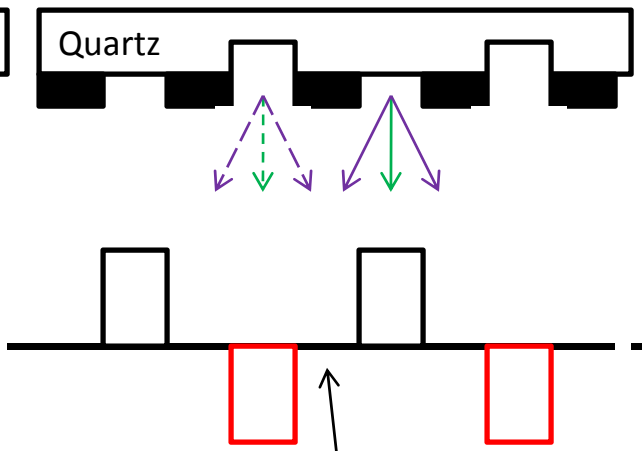


Here Light is transmitted and diffracted

Here transmitted light leaks into the area that suppose to be dark where it will create a **constructive interference.** So no line is printed.

Chrome

Alternating

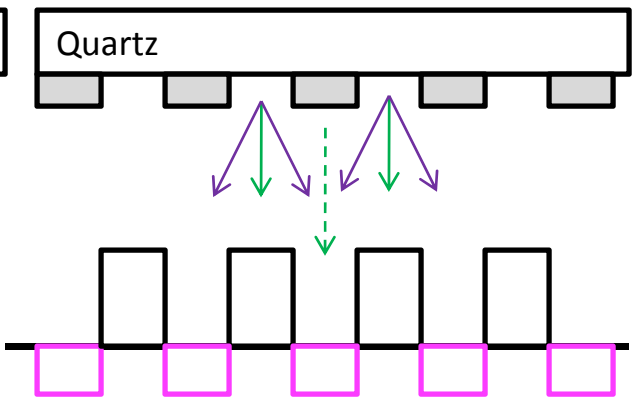


Here **destructive interference** creates a dark area where it will print a line

Here transmitted light is shifted **180°** due to etched quartz.

Chrome

Attenuated

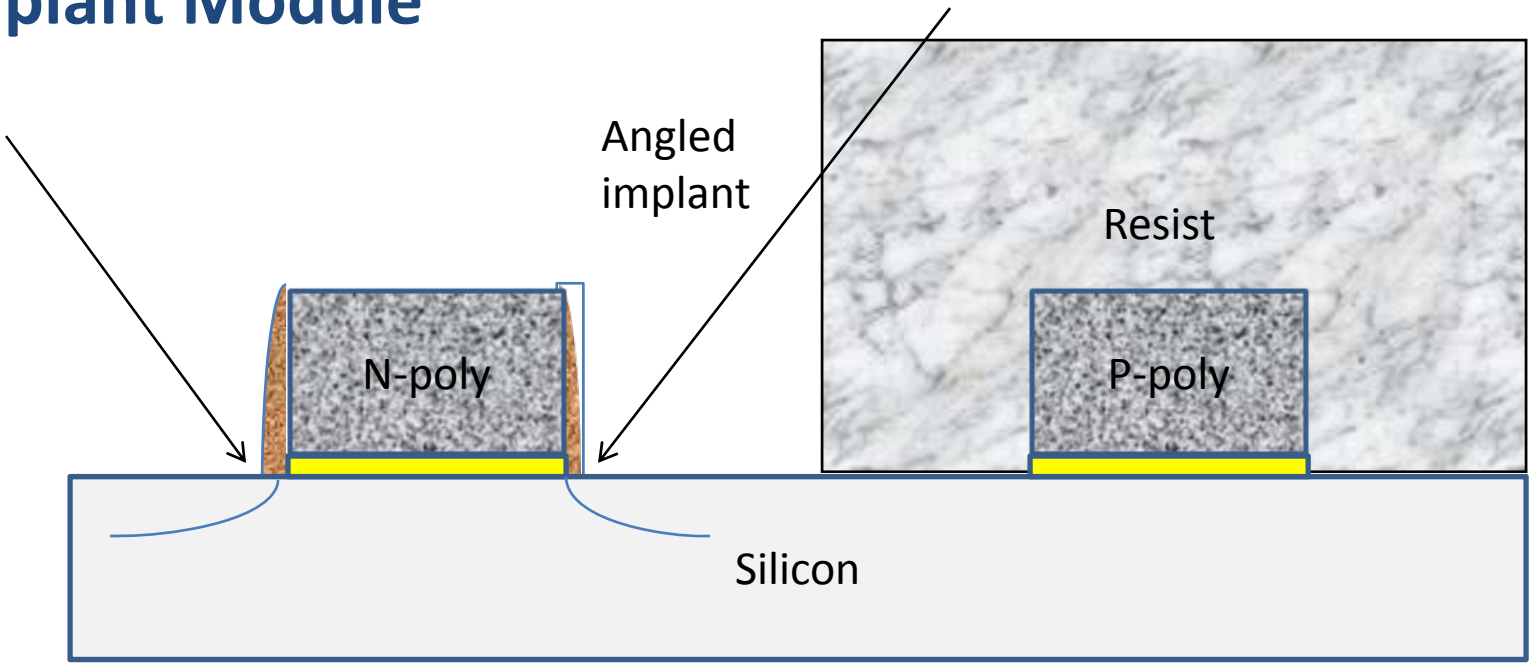


Here **destructive interference** creates a dark area where it will print a line

Here light partially transmitted (by selecting masking material and its thickness) and it is shifted **180° .**

MoSi

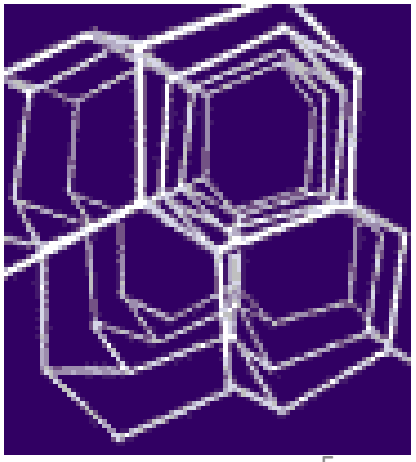
a. Implant Module



Problems:

a) Ion Channeling creates impl tail
   * 7-degree tilt
   * Pre amorphization imlp
   * Screening oxide
b) Substrate amorphization
c) Defects and dislocation

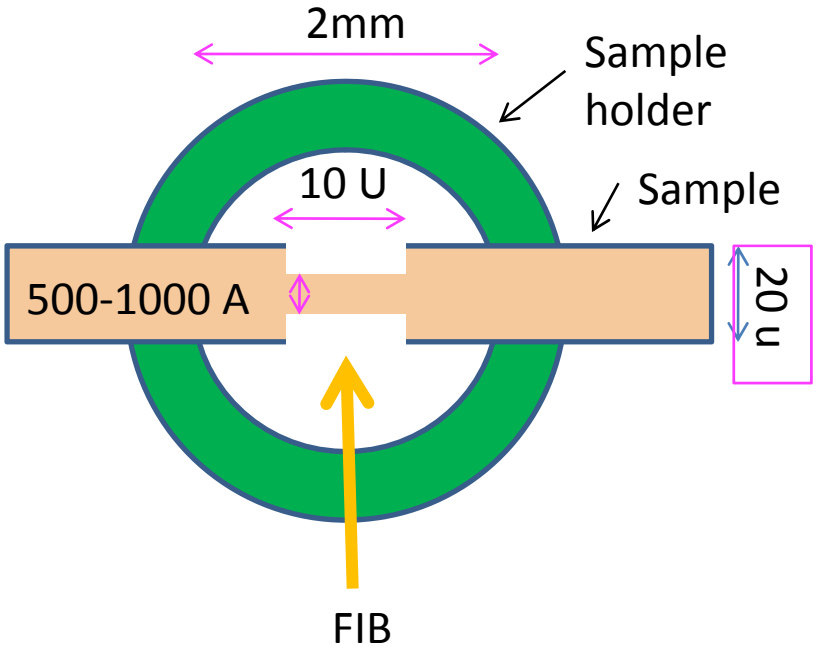
A diamond cubic crystal viewed from the <110> direction, showing hexagonal ion channels.
Source: Wikipedia



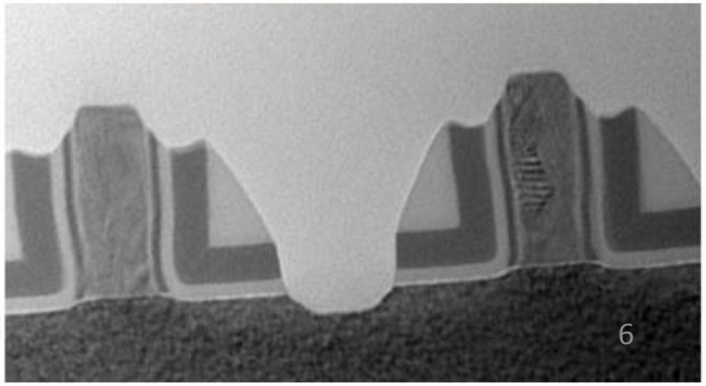
b – TEM (Transmission Electron Microscope)

Sample Prep:

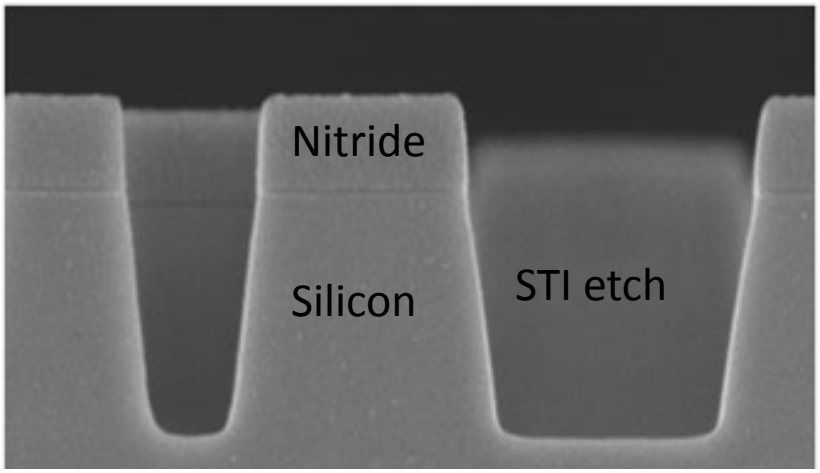
a) Use ion milling (Ga) to etch away silicon
b) Check under SEM
c) Cut a thin sample



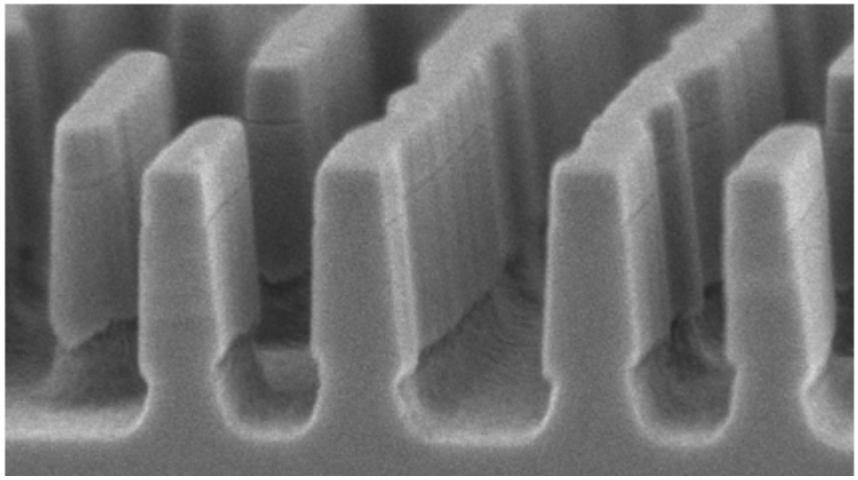
High energy electron beam transmitted through a very thin sample to image the microstructure of materials with atomic scale resolution



a - STI (Shallow Trench Isolation) + CMP



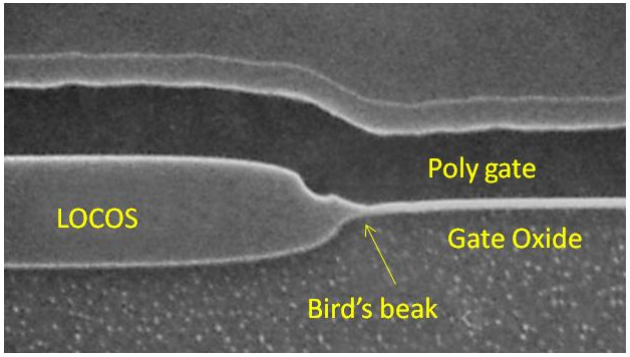
2-D TEM picture of STI



3-D TEM picture of STI

Why STI over LOCOS (Field Oxide)?

1) No waste of silicon due to bird's beak
2) Planar surface
3) Stress induced silicon dislocations



Local Oxidation of Silicon

c - Gate Dielectric / Poly

Gate CD bias reduction between PMOS and NMOS

For example, NMOS is doped with phos to reduce poly depletion and PMOS is un-doped

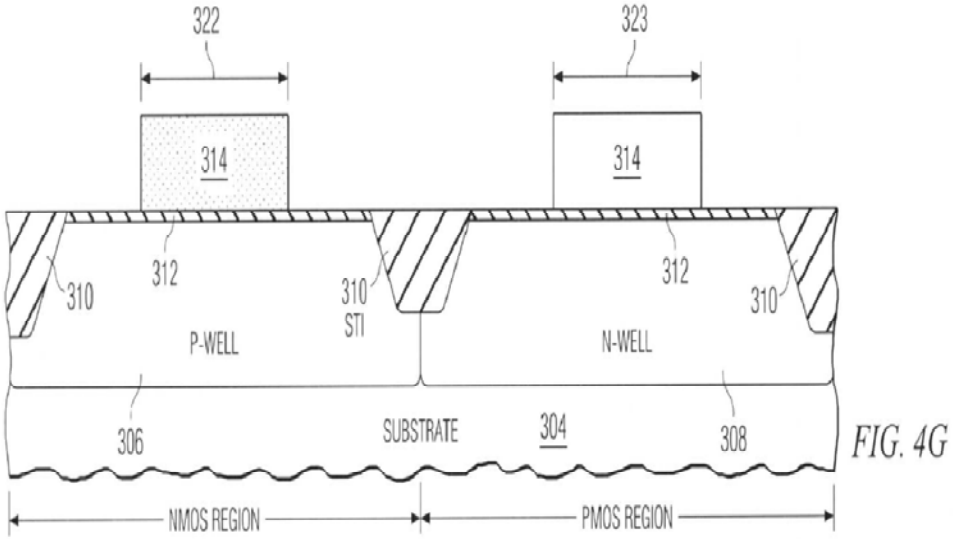
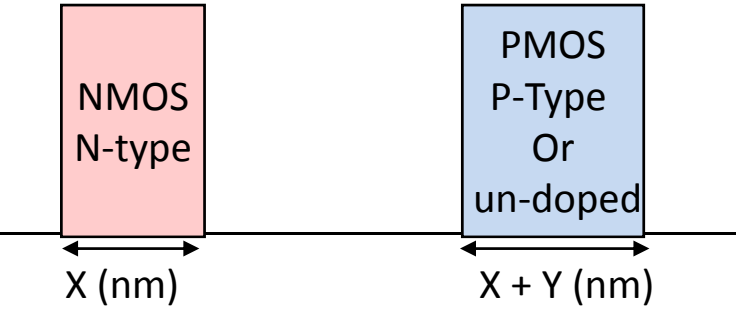
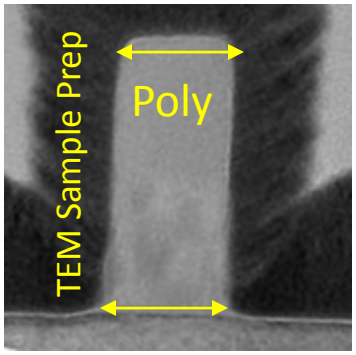


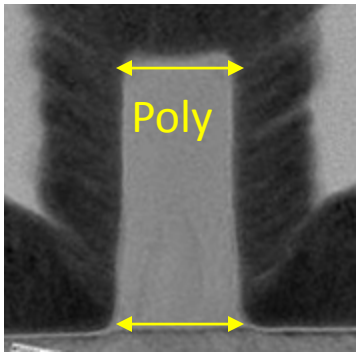
FIG. 4G

Implant "Si“ to convert the "Poly silicon" to "Amorphous Silicon. The extra implanted Si atoms will act just like the Si with no side-effects. But the gate etch process will see the effect of "amorphous poly" more than the effect of doping. Therefore there will be no CD bias between n-poly and p-poly.

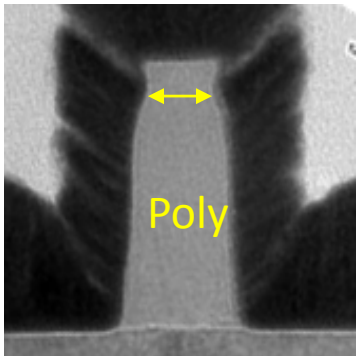




N-poly Impl + anneal + Si=1E15/20KeV



P-poly + anneal + Si=1E15/20KeV



N-poly Impl + no anneal + Si=1E15/20KeV

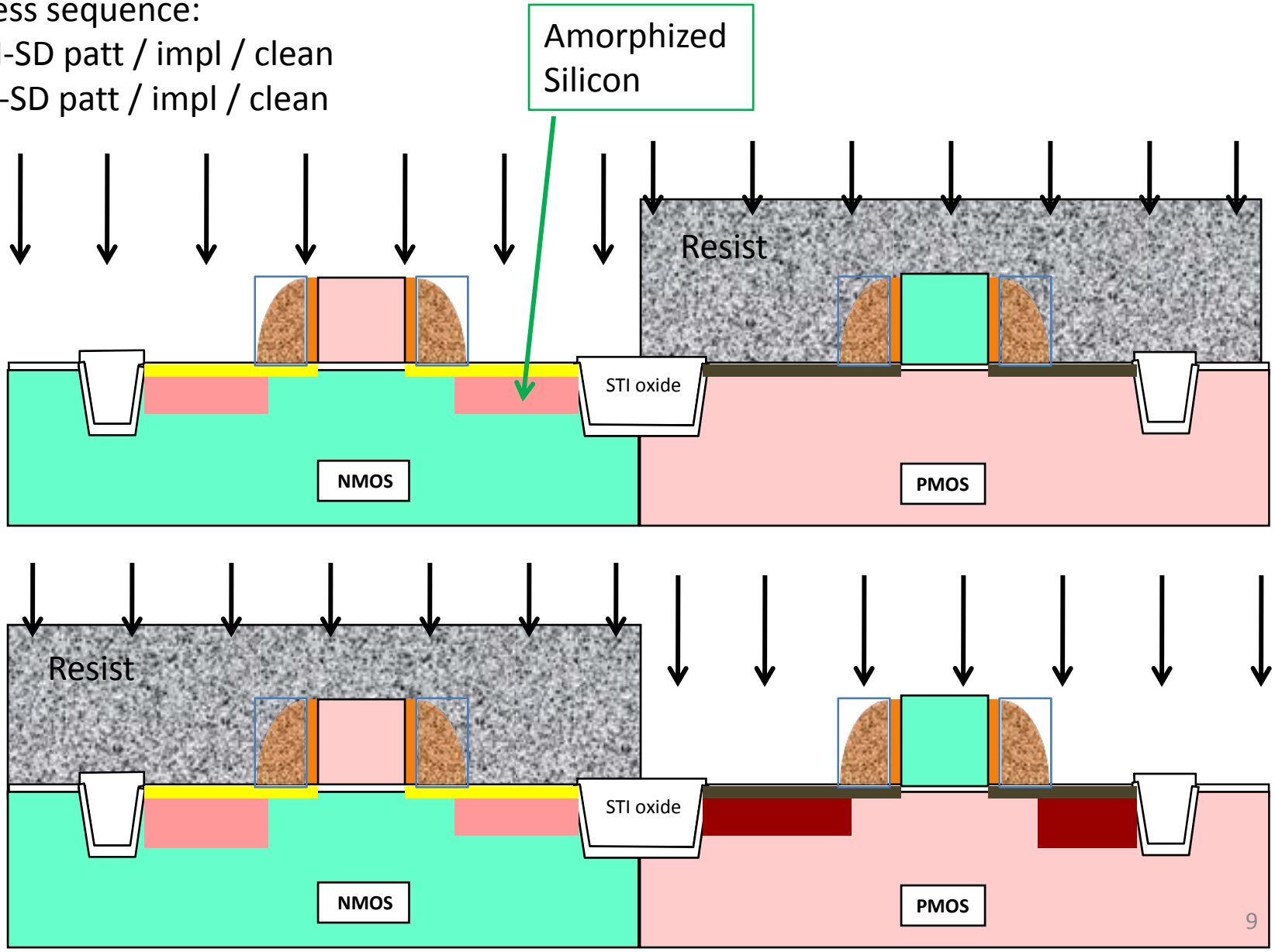
Source: Patent TI-64136

f – Source/ Drain

Process sequence:

a) N-SD patt / impl / clean

b) P-SD patt / impl / clean

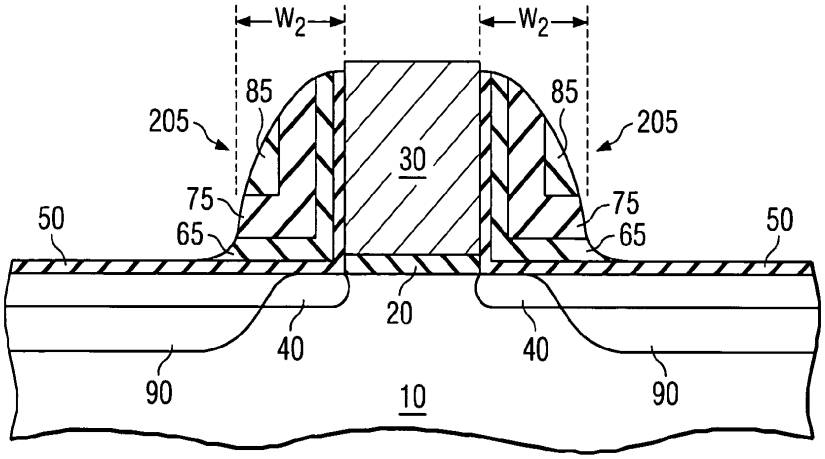


f – Source/ Drain

Issues:

(1) Harder to silicide narrow poly line
(2) SD impl might overrun the LDD
(3) Cont spacing to SW
(4) Diode leakage (Active silicide to Junction)

Solution:
Add a short "timed" dry SW etch post SD anneal



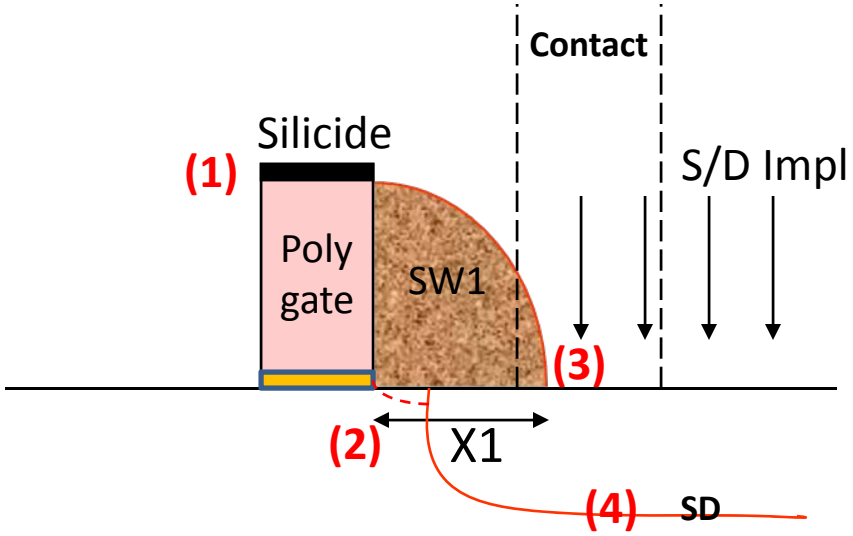


Fig. 1

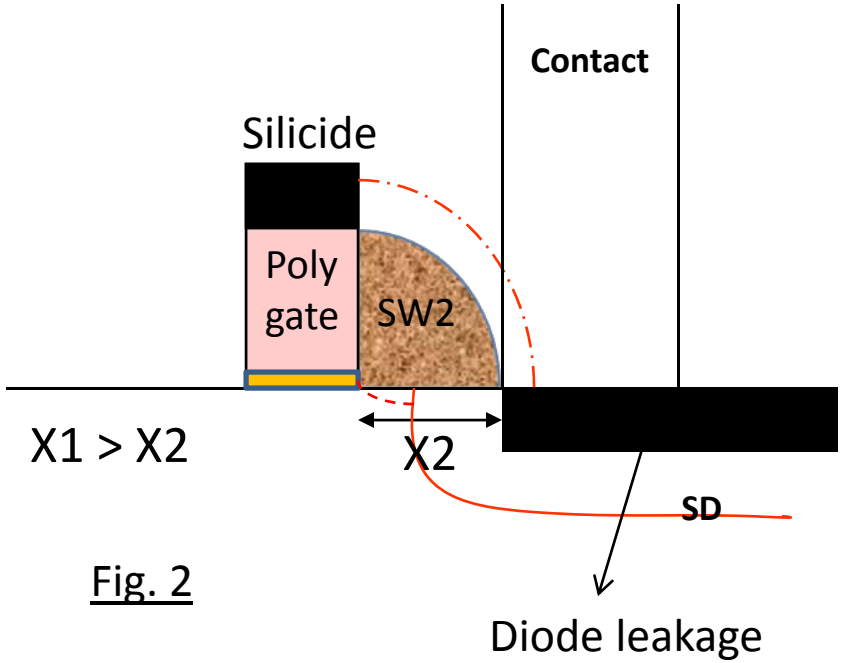
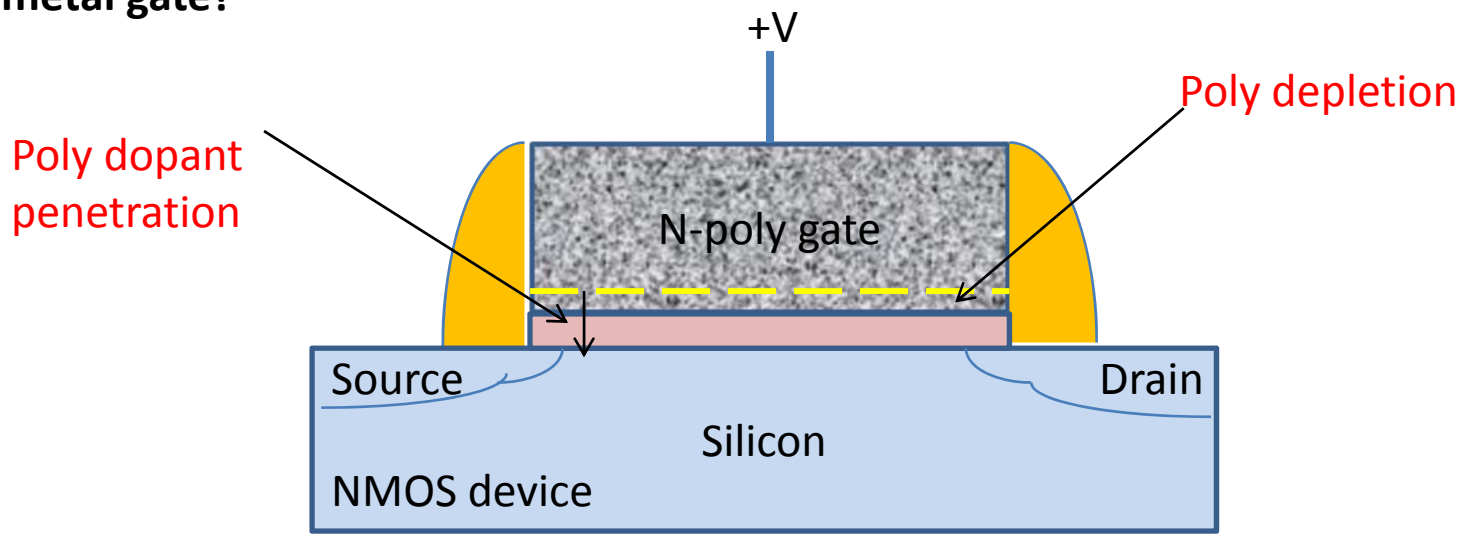


Fig. 2

Source: U.S. Patent 7,078,347

b – Metal gate

Why metal gate?



Poly depletion will reduce the gate capacitance where it will lead to less Charge in the inversion layer. This will reduce the transistor performance.

Issues:

1) Process integration complexity and cost
2) Getting the right work function for CMOS