ESD Design & Qualification for Integrated Circuits

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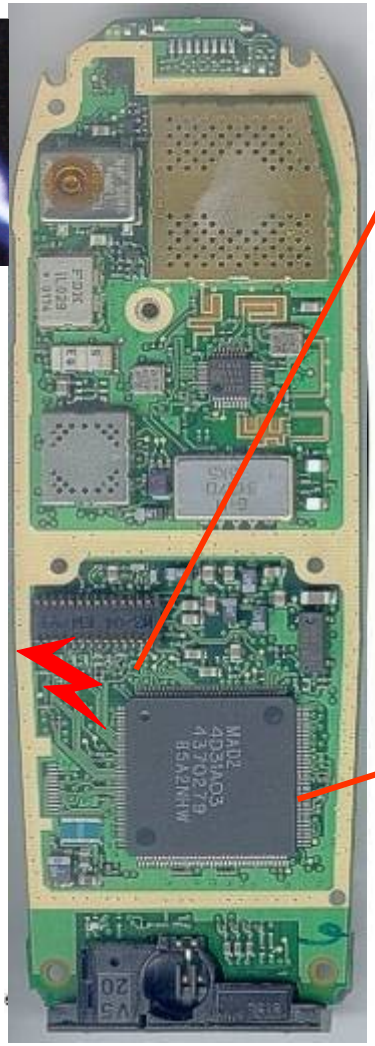
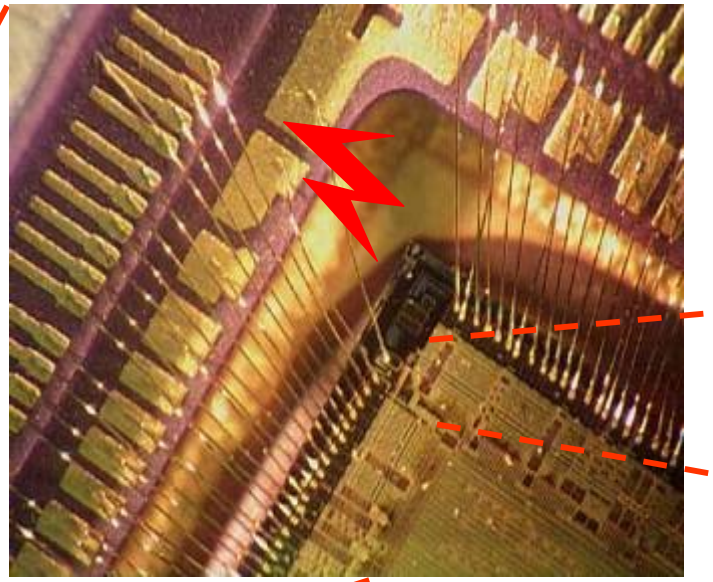
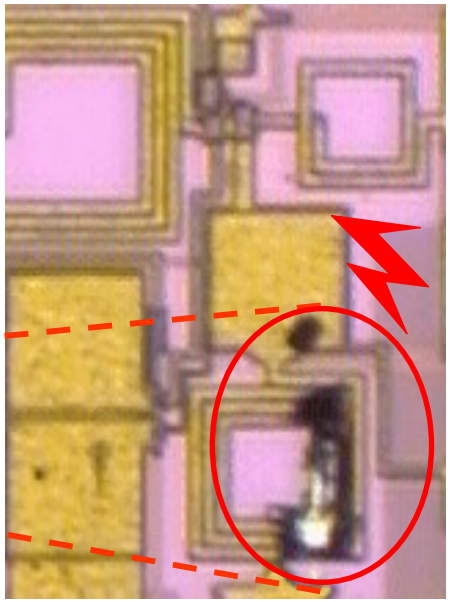
NOVORELL Technologies

ElectroStatic Discharge is everywhere…

ESD







power levels

circuit ~ 100mW ESD pulse ~ 10W

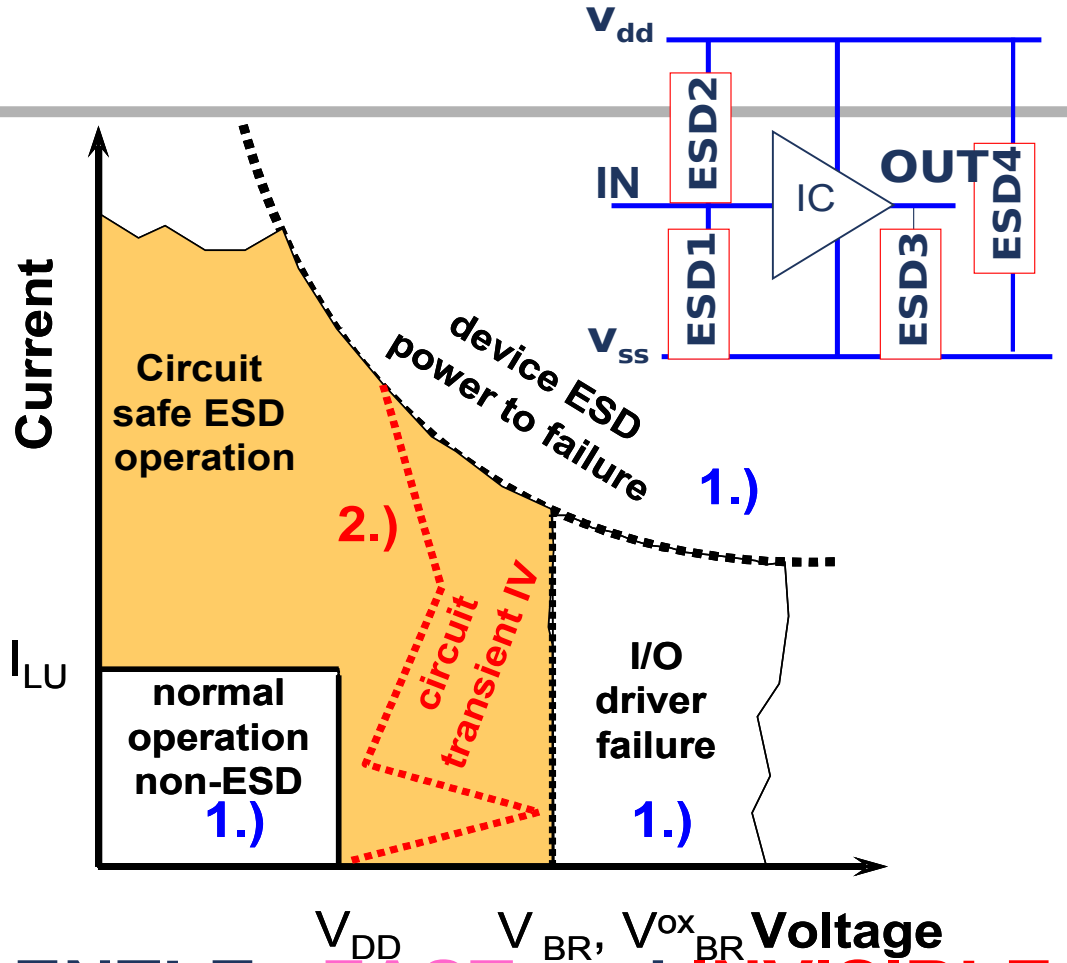
Δ ~ 100÷1000 times!

ESD is a major failure mode for the electronic equipment nowadays

IC OPERATING REGIONS:

1. Non-ESD operation – see figure : boundaries of the ESD design space/SOA
   - depends on technology and ESD structure design

2. **In ESD events, circuit transient IV must be within the SOA – region 2**
   - depends on ESD cell *AND* protected circuit performance and interactions

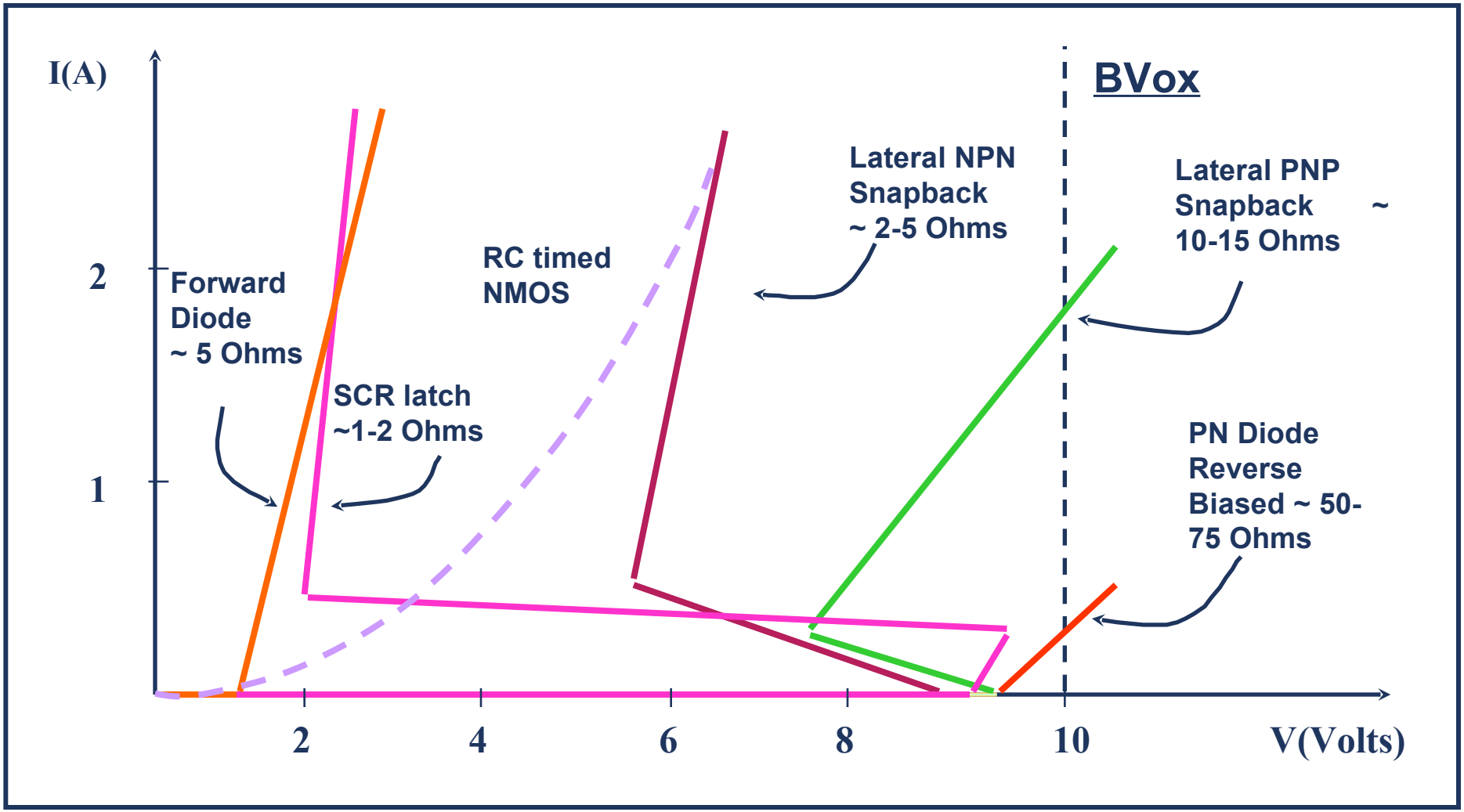


ESD device **: ROBUST, GENTLE, FAST and INVISIBLE**

: deviate the ESD stress from the IC

Every ESD clamp = **current switch**:
CLOSED in ESD, OPEN in normal conditions

PROTECTION CIRCUIT ELEMENTS

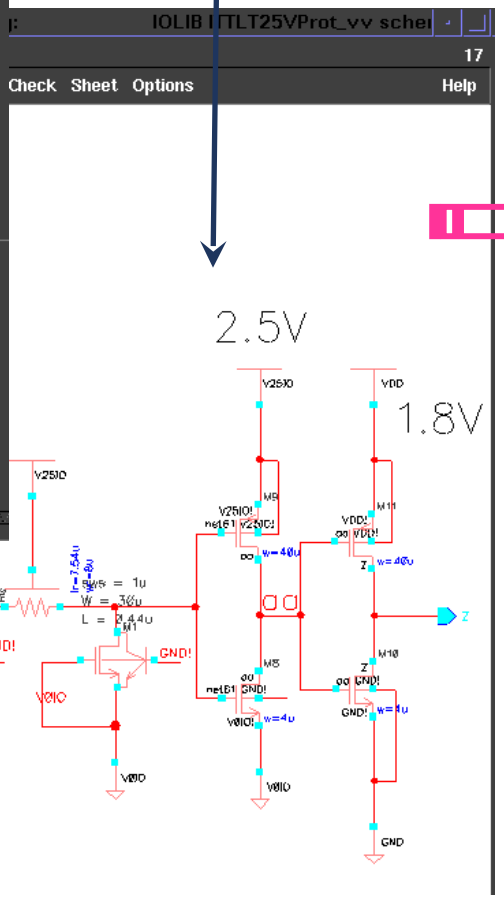


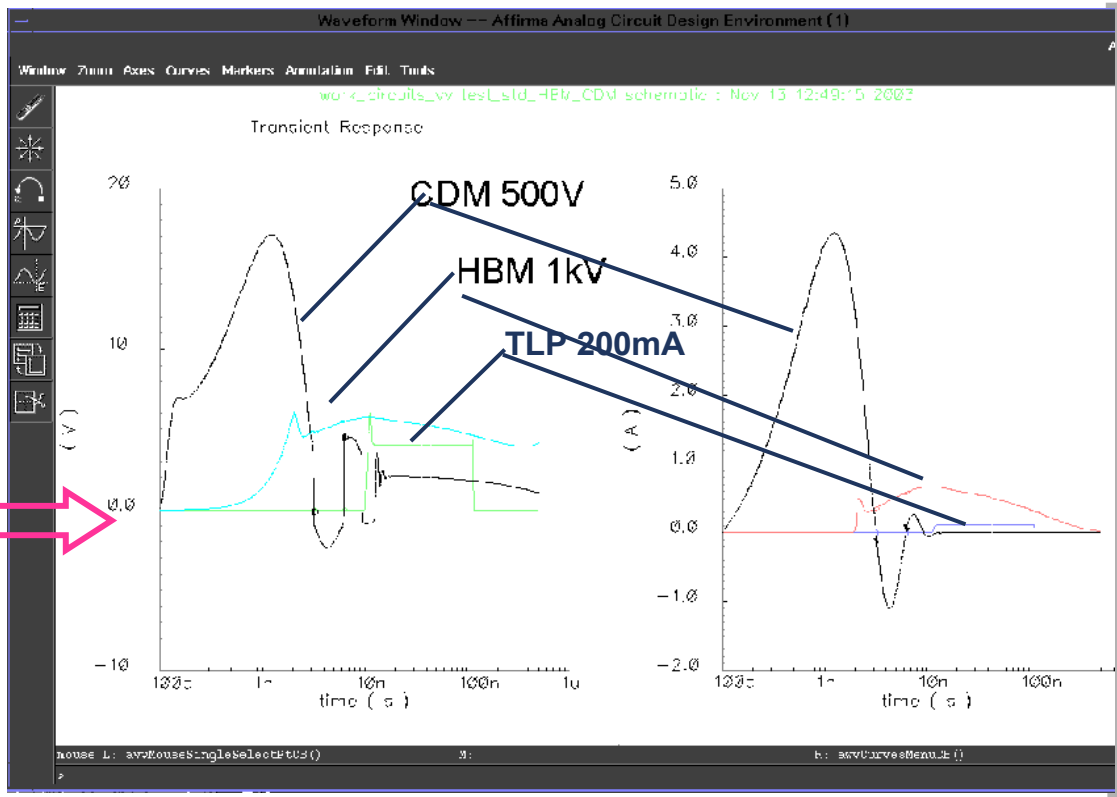
Any type of ESD clamp must protect the gate oxide with a breakdown of Bvox.

ESD design kit Implementation in Analog Artist/CADENCE

ESD model parameters

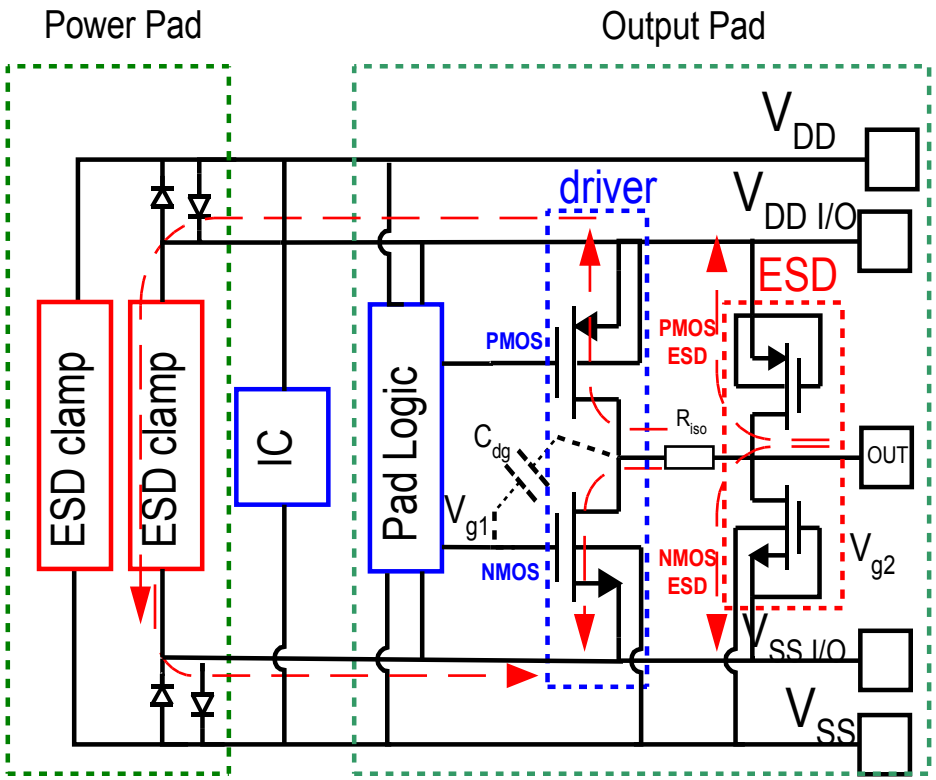
ESD components schematic views



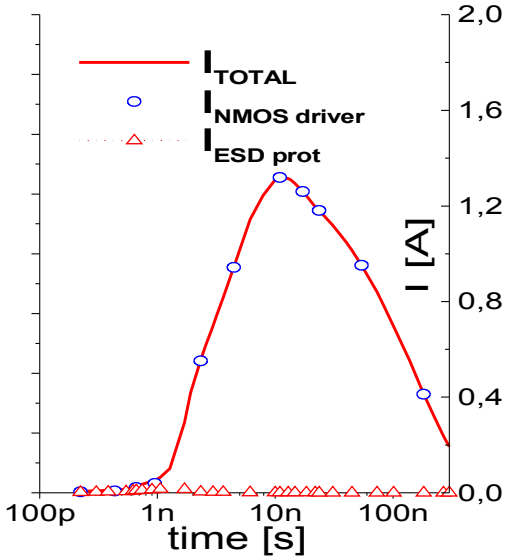


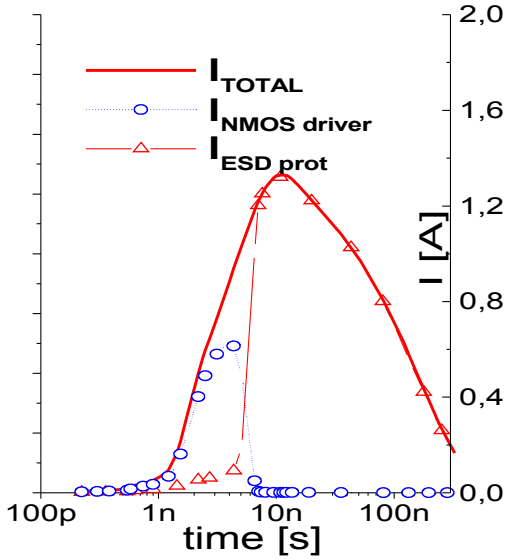
The ESD extensions of a given design kit with ESD models allows designers to simulate ESD and optimize the whole circuit

Optimization of the ESD protection in a digital Output Pad



2kV Human Body Model ESD stress between OUTPUT and VSS IO





Initial design (no gate coupling)

The ESD protection is too slow and does not activate, the output NMOS takes all the stress – not OK

Improved design (fixed RC gate coupling

The ESD protection activates OK and conducts all the ESD stress current after 10ns

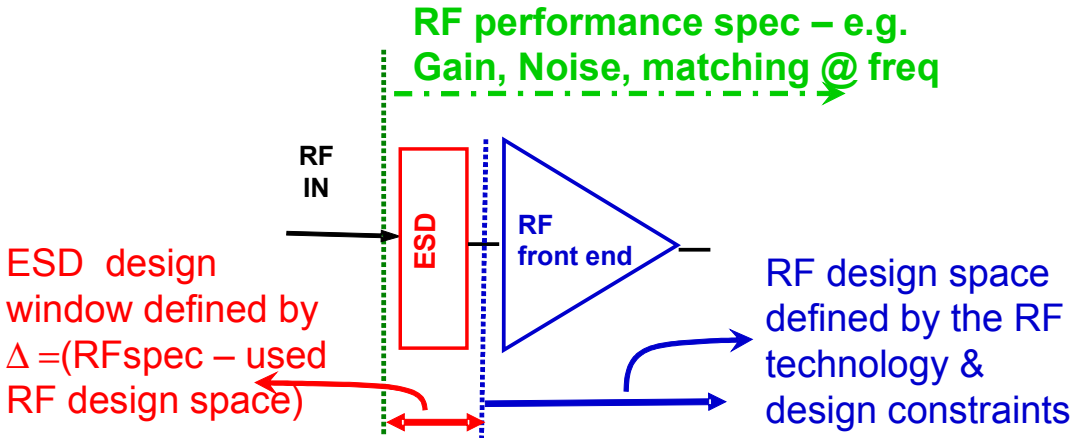
The use of ESD simulation enabled PDK allows to optimize and verify the operation of the ESD protection circuit prior design release

NOVORELL's ESD protection approach for RF I/O's

Two possible ESD-for-RF Design Methodologies

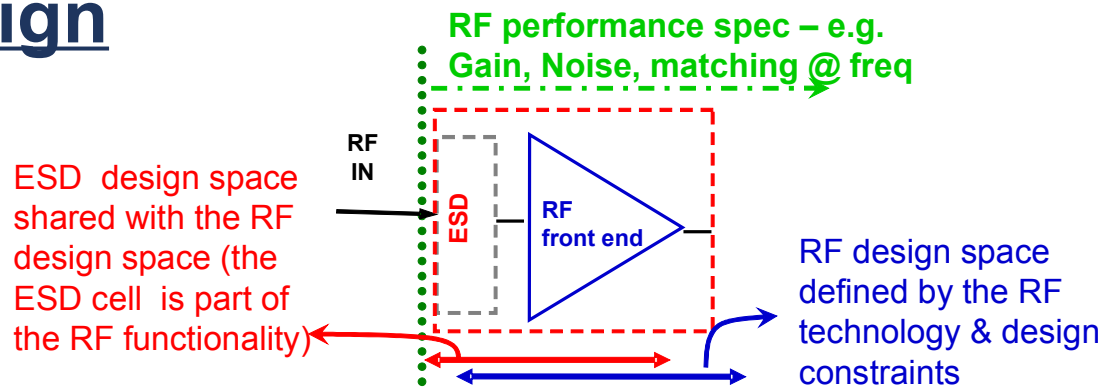
'Plug and Play'

independent RF and ESD designs; fit (shrink) ESD devices into the available RF design window to meet the RF specs; Limited ESD performance possible



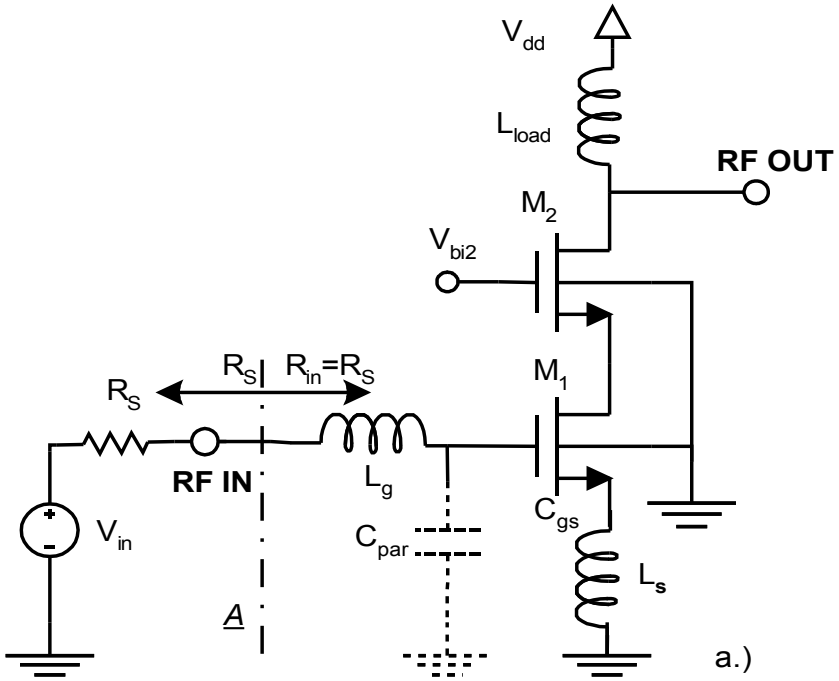
ESD-RF Circuits co-design

full circuit optimization; ESD structure is part of the RF design space, thus stronger ESD cell can be used. HIGH RF ESD specs can be achieved

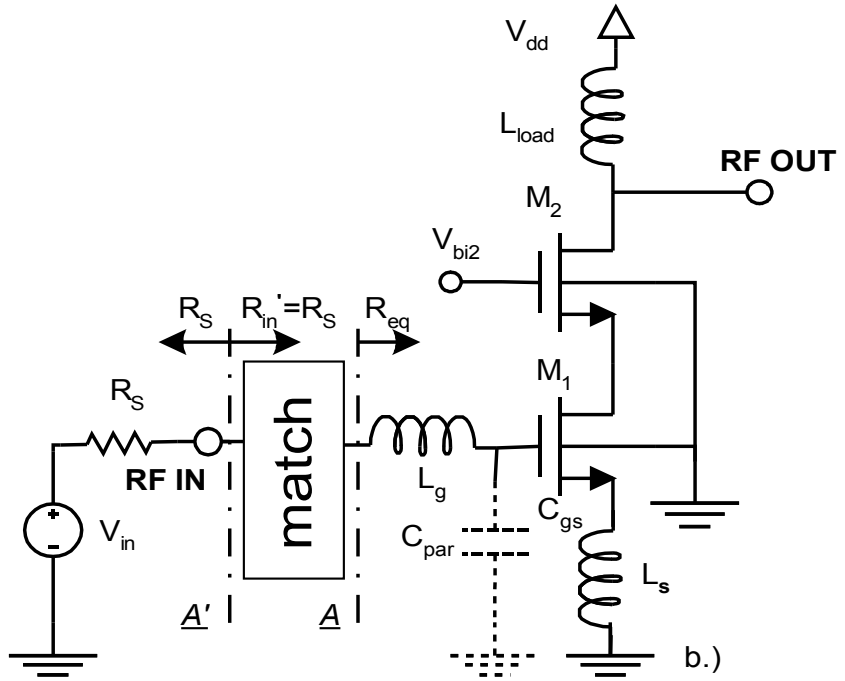


Depending on the design space and specific RF product spec, different ESD approaches are feasible

Generic common source LNA matching approach



direct match



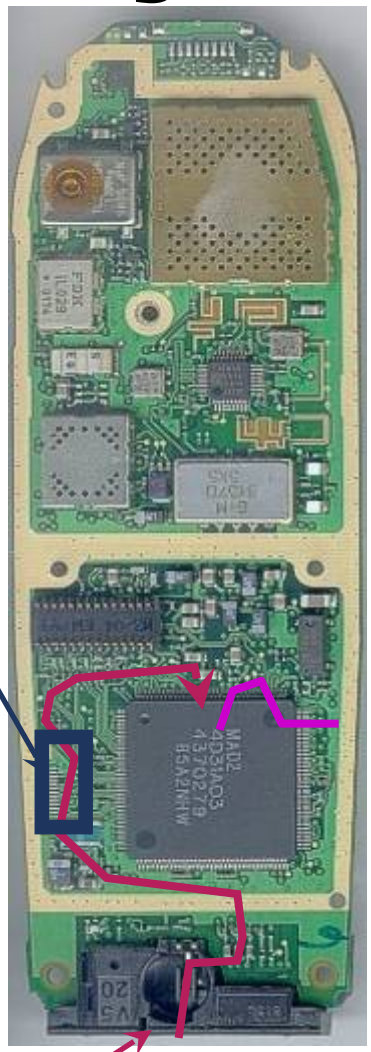
indirect match

The presence of the ESD device imposes an upper limit on the allowable Rin; power match is not always possible

$$R_{in}(=R_s) \leq \frac{1}{2\omega C_{par}(1+\frac{C_{par}}{C_{gs}})}$$

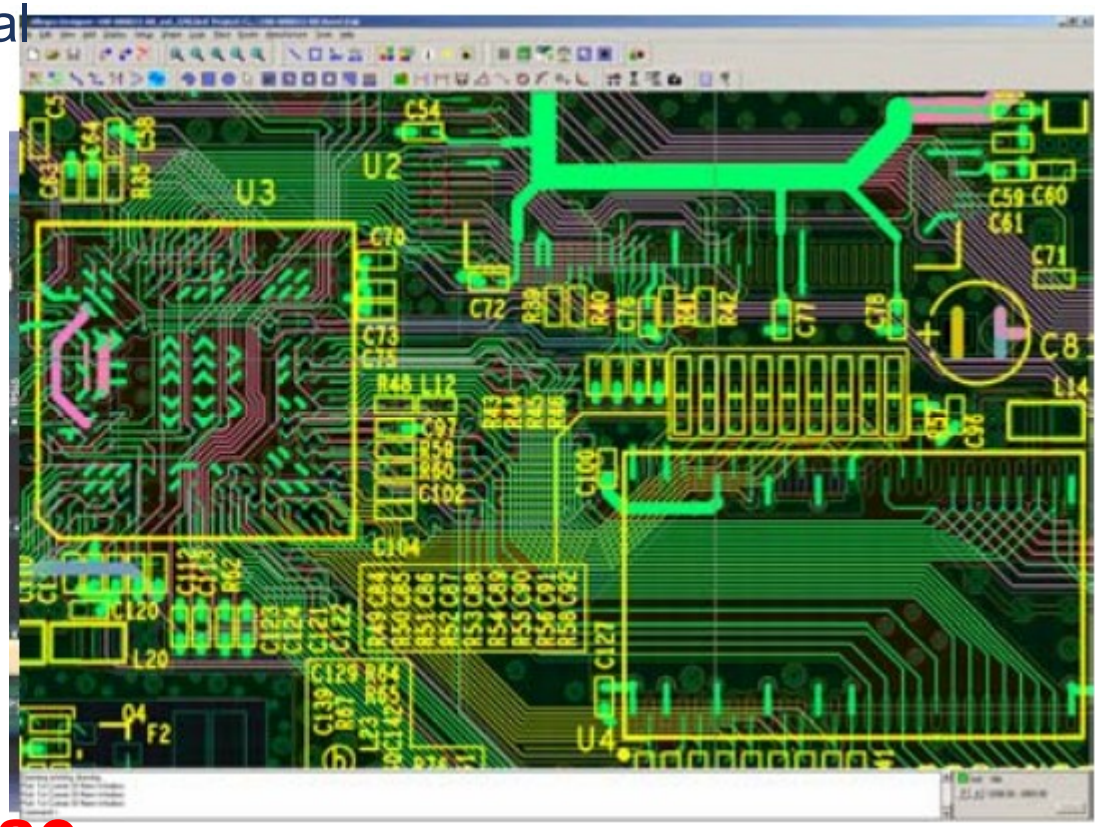
System level ESD design

The PCB board and discrete components act as filters which change in “unknown’ way the input waveform

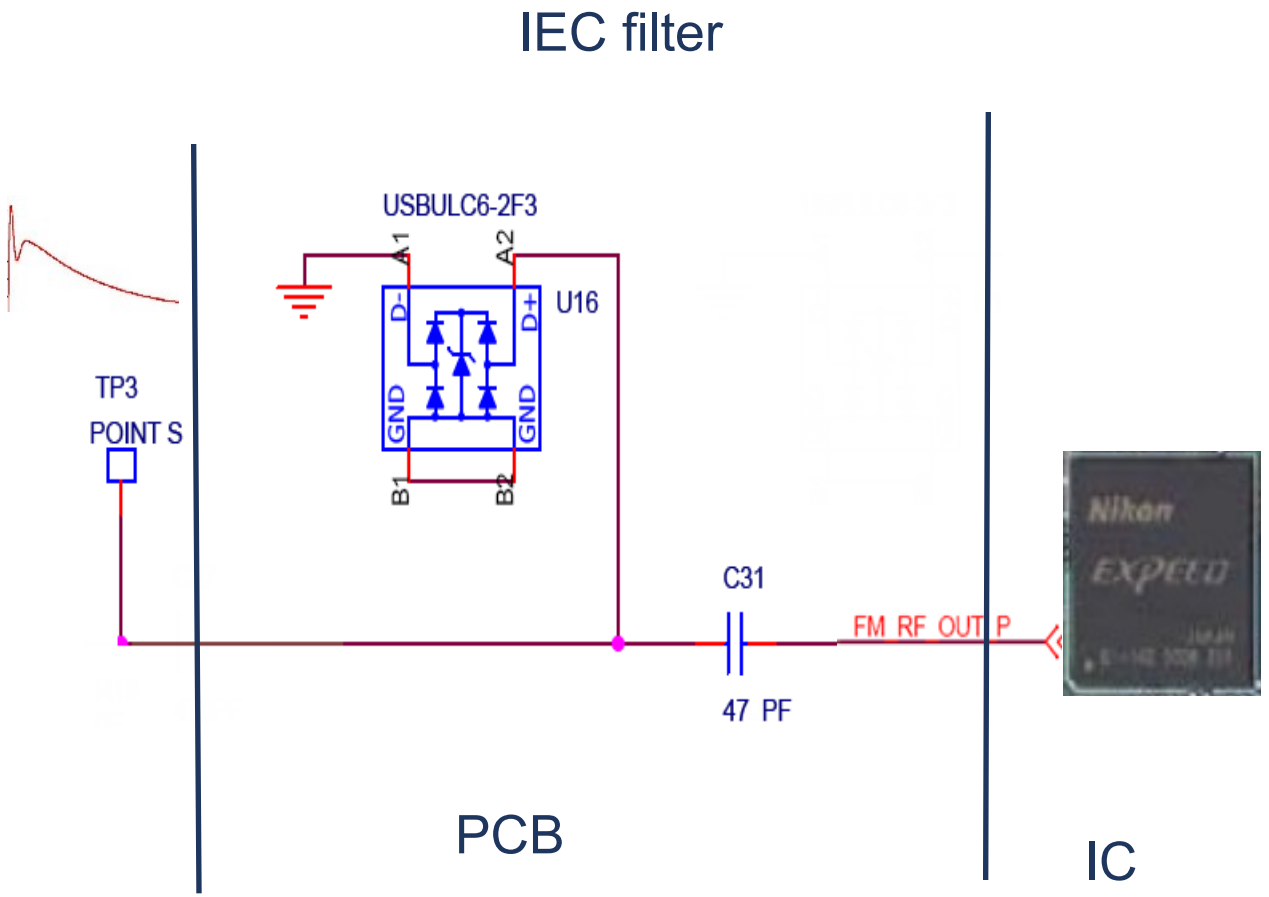


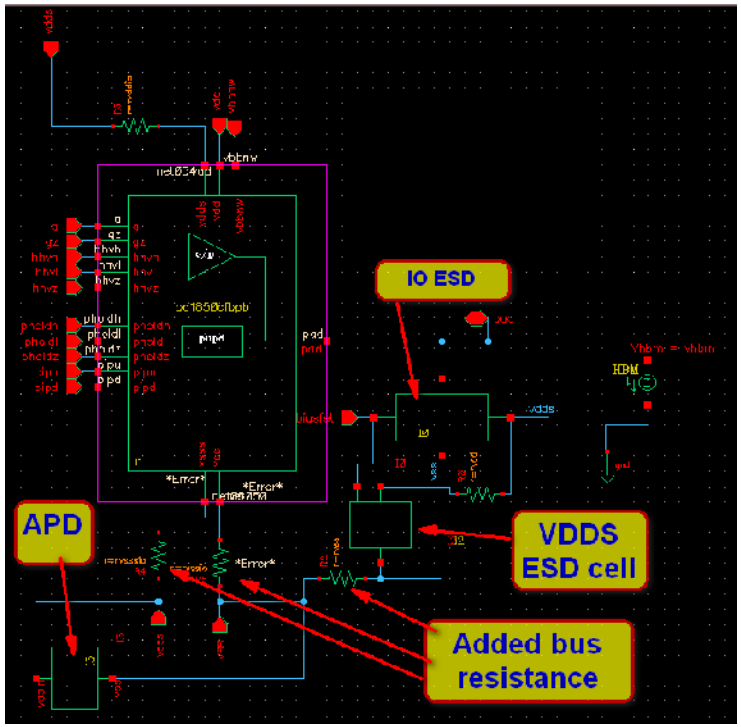
IEC ESD pulse

- Large Voltage transients can occur inside the PCB board
- ESD IEC waveform on IC - **Not** defined !
- Use discrete components to filter input IEC signal



IEC Protection design = IC + PCB co-design!





Cell Level ESD Checks

- Verify that correct version of the device/design kit/cell/library is being used when using standard library cells or parameterized cells (PCELLs).
- Verify compliance of individual and multiple cell devices with ESD geometrical rules.
- Verify ESD protection element between I/O and power (VDD, VSS) rails, including correct device polarity, within I/O cell.
- Verify power clamp between power rails (VDD, VSS), including correct device polarity, within I/O or supply cell.
- Verify trigger circuit implementation in transient-triggered designs.
- Verify termination cell implementation.
- Verify interface cell implementation.
- Verify device rating compliance in cell implementation.
- Verify robustness of metal lines and interconnects along the ESD protection discharge path.
- Verify compliance of extracted metal resistances of the paths within the cell with allowed design limits.
- **Verify implementation of secondary ESD protection scheme**