INTRODUCTION TO SYSTEM VERILOG

For Design and Verification Engineers

WHY SYSTEM VERILOG

- Newest revision of IEEE standard Verilog
- Many features to benefit design and verification engineers
- Support for higher levels of abstraction
- More easily understood code
- Integration of verification and design into single language
- Integration of coverage metrics
- Integration of an assertion language

WHY THIS COURSE?

- Focus on most useful features to enable highest ROI
- Learn how and when to incorporate new modeling techniques into your designs
- How to leverage System Verilog covergroups to facilitate coverage measurement.
- How to create simple assertions to check interface assumptions and to enable white box checking of your designs
- Real-world examples

SYLLABUS

Design hierarchy
- Package declaration and use
- Nested modules
- Enhanced port connection syntax

Data types
- New data types and enumerated types
- Arrays and structs

Enhanced Literals
- Integer and logic literals
- Struct and array literals

Procedural blocks
- Sequential and combinational procedural blocks
- Task and function enhancements
- Reference arguments

Programming statements and operators
- New operators
- Enhanced looping constructs
- Unique and priority decision statements

System Verilog Interfaces
- Interface definition and use
- Defining module ports and directions

Assertions
- Concurrent assertions and sequences
- Disabling assertions during reset
- Assertion messages

Coverage
- Coverage concepts and statements
- RTL coverage versus functional coverage

WHO SHOULD ATTEND

- Digital designers looking to upgrade their skill set
- ASIC designers looking to understand how System Verilog features can positively impact their designs
- EDA Methodology / Flow engineers who want to understand how adopting System Verilog can enhance their methodology.
- Engineers from startups or smaller design companies who are responsible for several phases of work.
- Verification engineers who want to understand System Verilog hardware modeling extensions or who want to influence the direction of RTL design to higher abstraction levels.

INSTRUCTOR

- 16 years EDA, IC design, and verification industries
- Founder and CEO, Hyper Analytix.
  - Chief architect and lead engineer for declarative verification tools.
  - Lead consultant for Convey Computer and Ikanos Communication ASIC verification contracts.
- Senior Architect, Cadence. R&D lead formal and simulation based verification tools.
- CTO, Nucleus Logic. Lead architect and project lead for Core-Logic-Network-Acceleration ASIC.
- Senior Engineer, Digital Archway. Verification lead for TCP/IP offload engine
- Senior Engineer, HP. High-end server ASIC physical and logic design.
- Senior Engineer, HP/Intel. Microprocessor design, verification, and physical design.