Problem Statement

In today's process technologies interaction and coupling between devices, circuit blocks and subsystems built on the same Si substrate are increasing dramatically (L, tox ↓, V ↓, Integration↑)

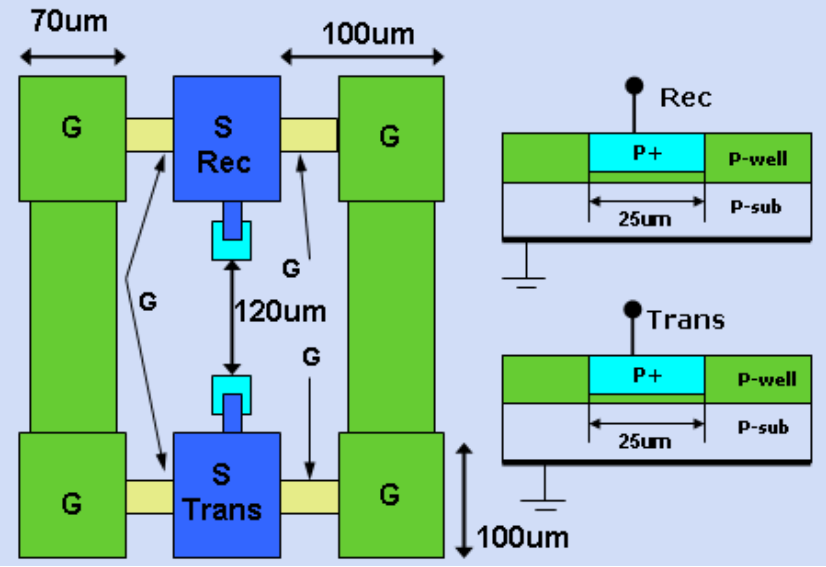
Such interaction causes undesirable interference signal to couple **via the Si substrate** from noisy switching circuits to sensitive low noise blocks causing performance degradation and yield hit.

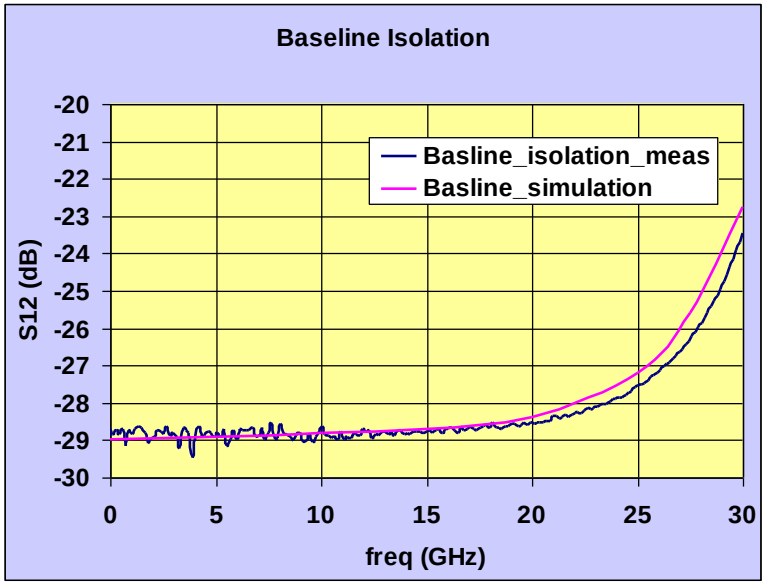
Substrate noise isolation is an increasing challenge in today's desirable SOC realizations

For RFIC and SOC, how can a quantitative Substrate noise coupling analysis methodology and design guide be provided as a part of the design, validation and debug environments rather than the "build it and see" mentality, when it is too late

1. Baseline Isolation

- Both the receiver and the transmitter have ohmic contact to the substrate, the substrate will behave as a resistive network up to the cutoff frequency
- The equivalent model between the receiver and the transmitter is all resistive and the S12 data is constant up to ~ 15GHz.
- Beyond 15GHz the isolation starts to depart from a resistive behavior due to the contribution of the distributed RC network that will now represent the substrate.
- The simulation results match the measurement up to 20GHz by tuning the psub doping concentration

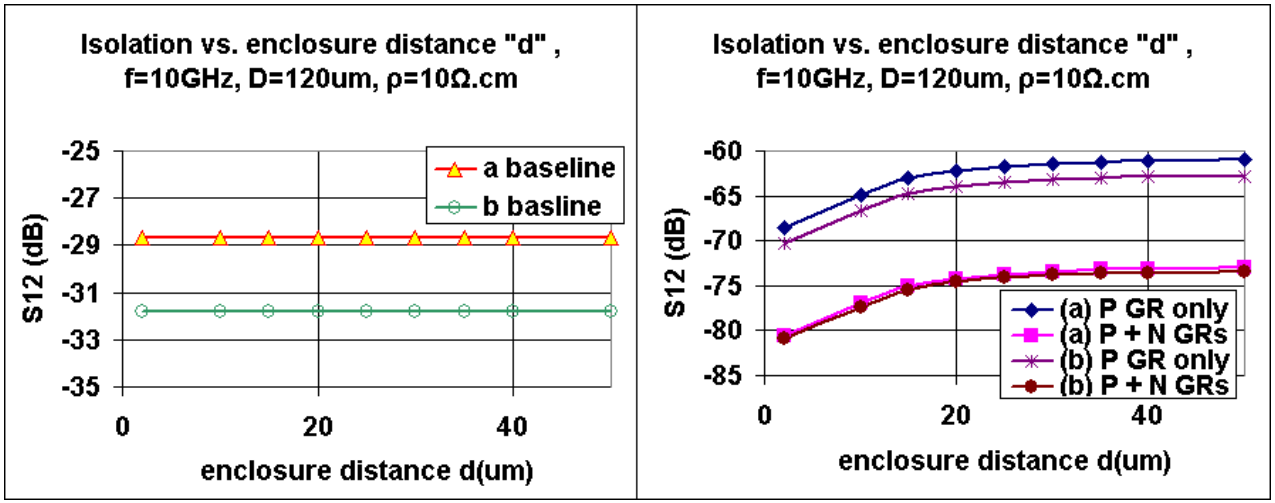


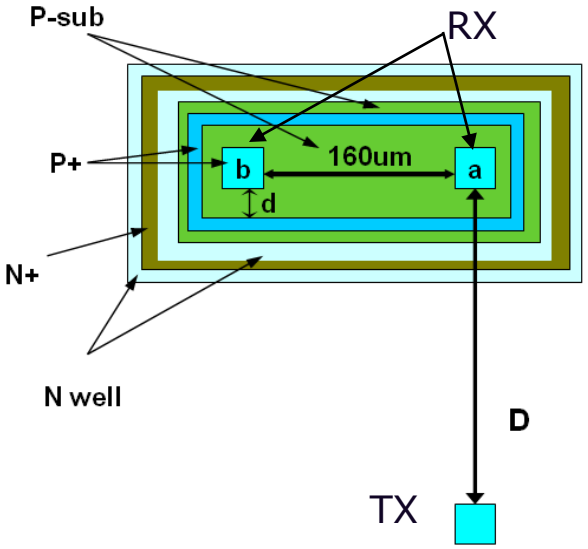


Differential Noise

- Differential circuits are always recommended over single-ended circuits in noisy environments, substrate noise is not an exception.
- The noise, due to its random nature, appears as a common-mode signal on the differential outputs.
- The delta in the isolation numbers of noise receiver a and b in the case of the baseline isolation is 3.1 dB. The delta is 1.78 dB in the case of a p guard ring only surrounding the noise receivers and 0.43 dB in the case of a dual guard ring.

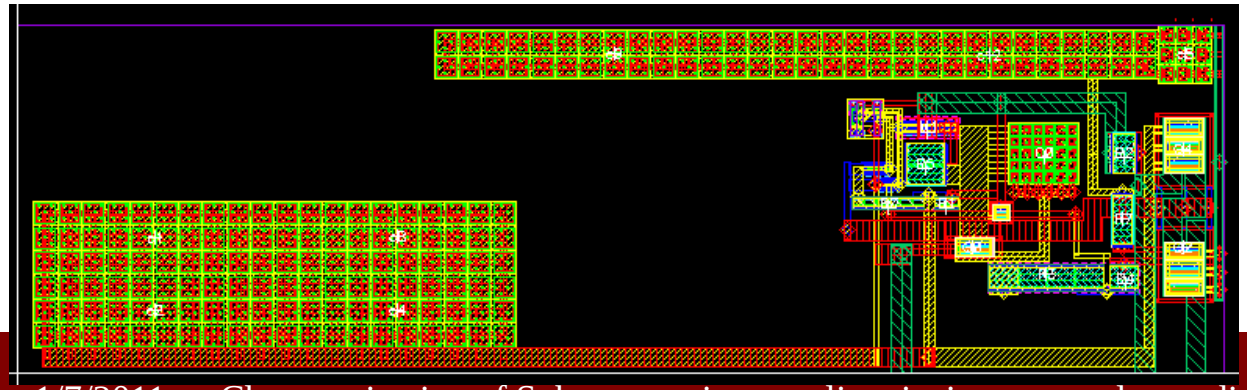
Design Guide 31: A dual guard ring when used for differential configurations, equalize noise coupling on the two sides of the differential structure and decrease the differential noise if compared to the p guard ring alone.

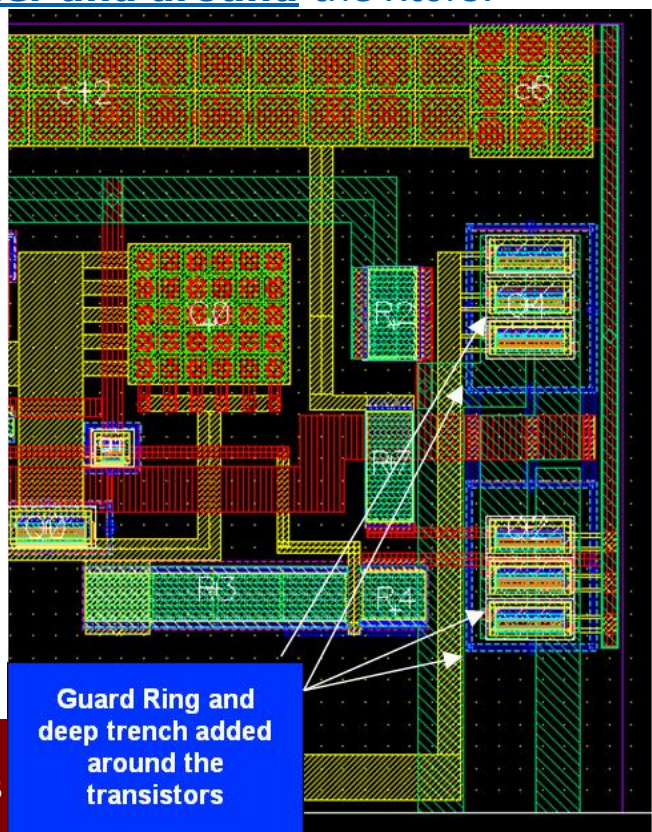




Circuit Level Case Study

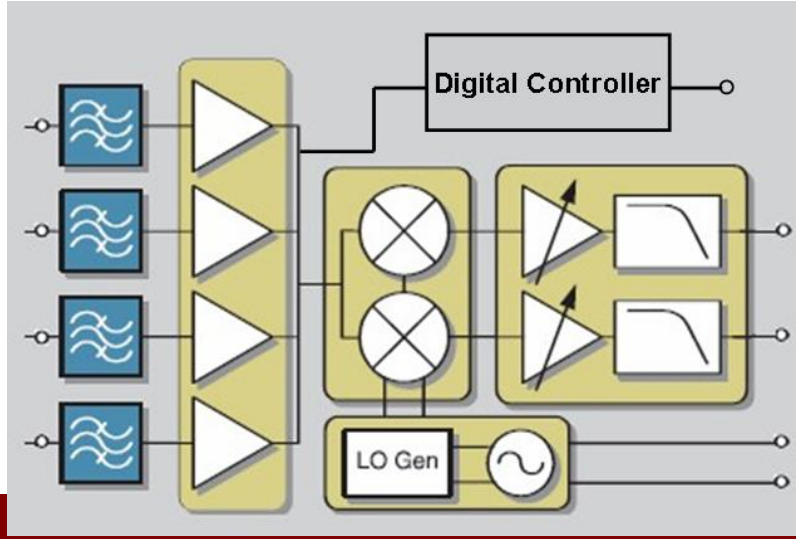
- Next the phase noise of the transmit buffer is analyzed w/ and w/o the sub network
- The thermal noise of the substrate resistive network acts as a white noise source that raises the phase noise floor of the TX buffer.
- Without layout modifications, the PN simulation **with** the substrate model shows the failure of the PN to meet the spec (-140 dBc/Hz @ 20MHz offset).
- The substrate behavior is modified by editing the layout to increase the value of resistors R1 to R5 **by the addition of a grid of deep trenches under and around** the xtors.
- This has the effect of increasing the distance between the devices and the substrate bulk; hence it increases the effective substrate resistance.
- In addition a GR is added around each transistor that will reduce the bulk current which in effect increases the bulk resistances.



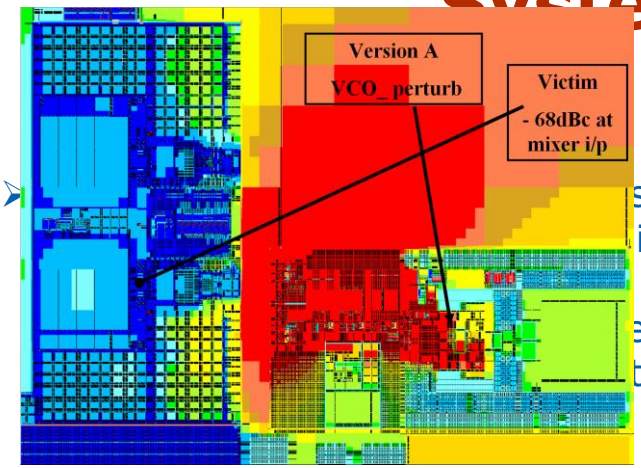


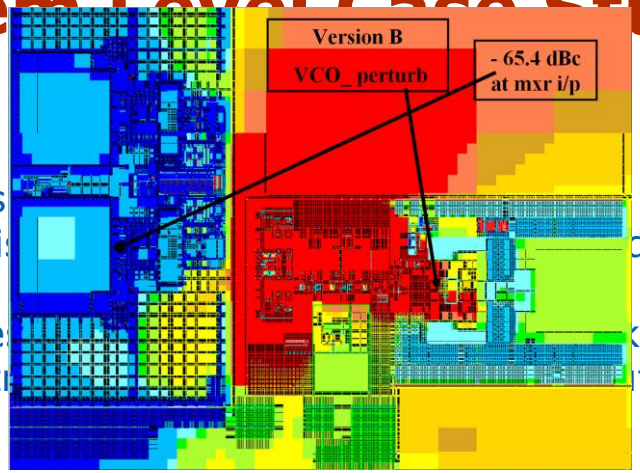
System Level Case Study 3

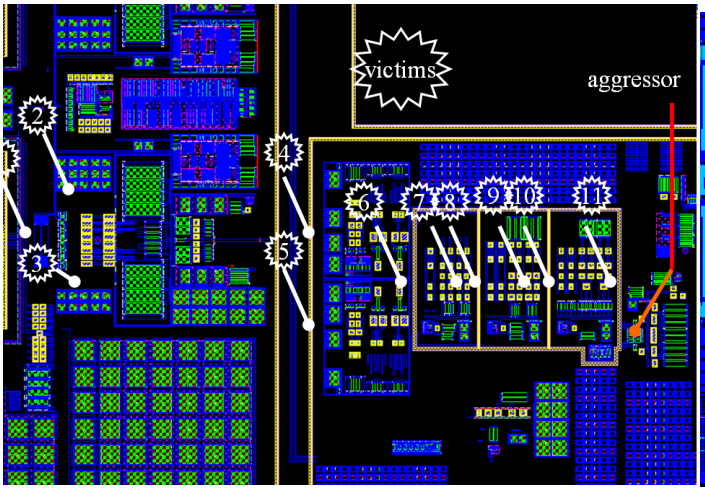
- In this example the substrate design flow is used in the debug phase of an industrial problem
- The system under study is an EDGE GSM cellular receiver shown below
- Two Si versions of the chip are available: Version B (the modified version) is meeting all block specs (per the breakouts measured data) but failing the C/N (carrier to noise) in the presence of a strong CW (continuous wave) blocker signal 3MHz away from the carrier at the high band (1.9GHz).
- Version A is failing some block specs, while passing the blocker C/N system spec
- **The goal of this study is to use the substrate noise coupling design flow and the developed design guide to analyze the signal coupling through the substrate for the 2 versions of the chip, and look for discrepancies that may explain the different blocker performance, then provide a solution for the problem to pass the system spec without impacting other specs**

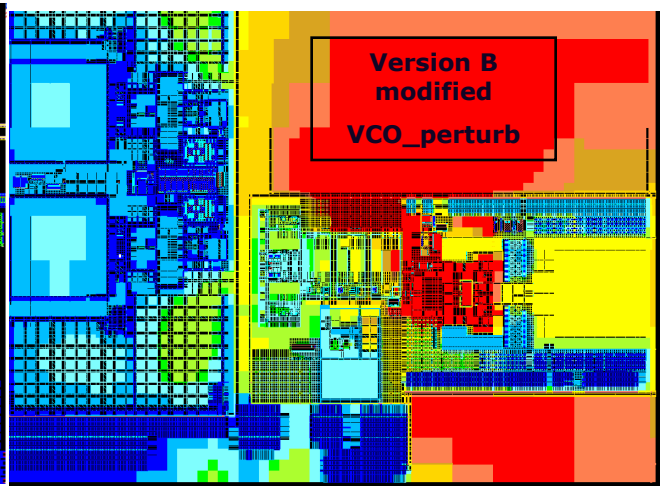


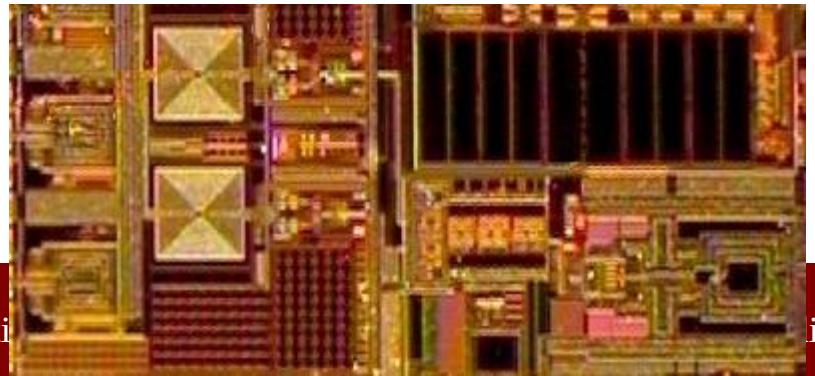
System Level Case Study









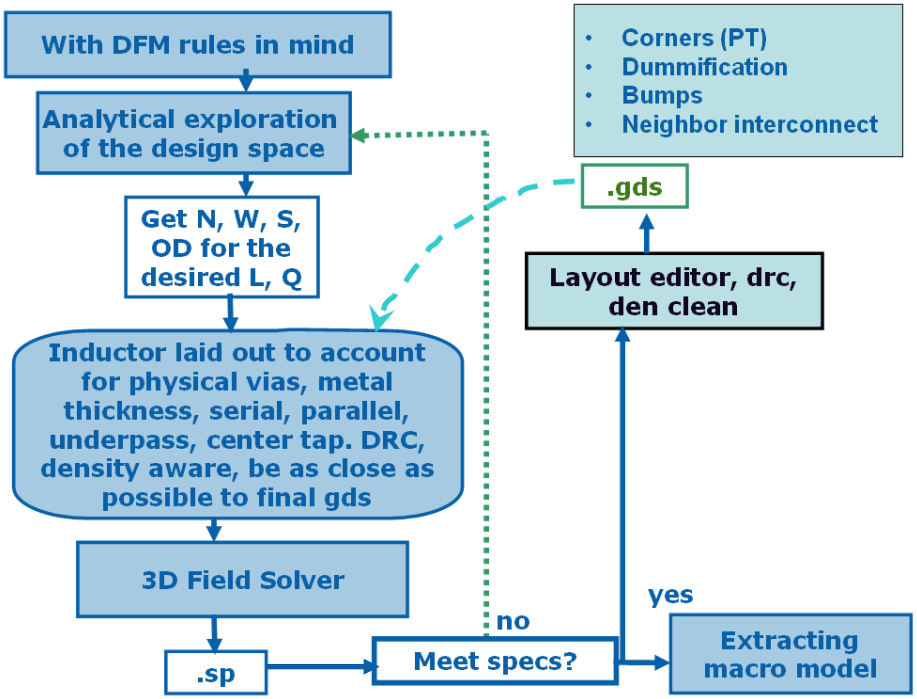


Victim points	*Version A*	*Version B*	*Modified version B*
1	*-68*	*-65.4*	*-71.8*
2	*-68.1*	*-66.2*	*-70.6*
3	*-68.4*	*-66.3*	*-70.3*
4	*-41.9*	*-37.8*	*-54.8*
5	*-41.7*	*-37.7*	*-54.7*
6	*-41.6*	*-36.3*	*-53.6*
7	*-41.1*	*-27.8*	*-52.4*
8	*-41.1*	*-27.9*	*-52.3*
9	*-40.9*	*-18.8*	*-50.4*
10	*-40.9*	*-18.8*	*-50.3*
11	*-16*	*-10*	*-41.4*

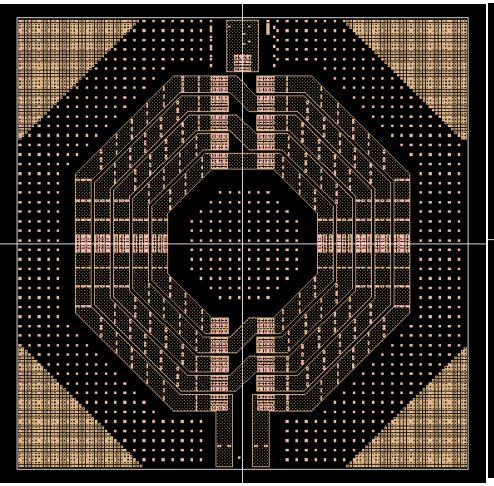
On-Chip Inductor Design Flow

- The flow starts by defining the inductor specification.
- Table below lists the entire set of the parameters that should be taken care of during designing the inductor.
- The list is extended to accommodate important DFM parameters that affect the inductor yield and render the inductors production worthy.

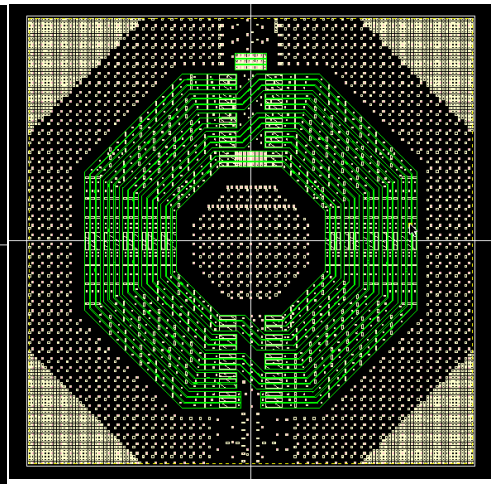
Inductance L
Desired minimum quality factor Q at the operating frequency fo
The operating frequency fo
Minimum self resonance frequency fr
Maximum DC current
Maximum rms current
Bump pitch for flip chip
Maximum metal density rules
Metal design rules, maximum width, minimum width, minimum spacing



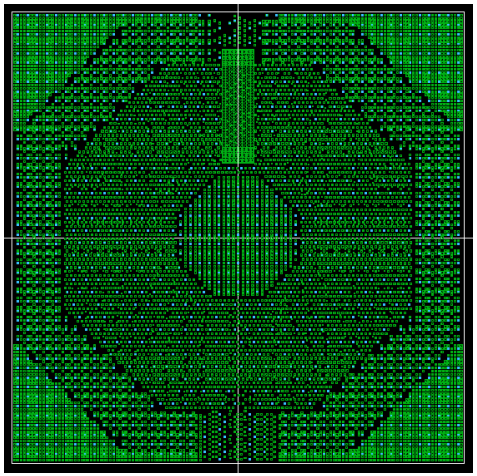
DFM Effects (Impact of Dummy Fill)



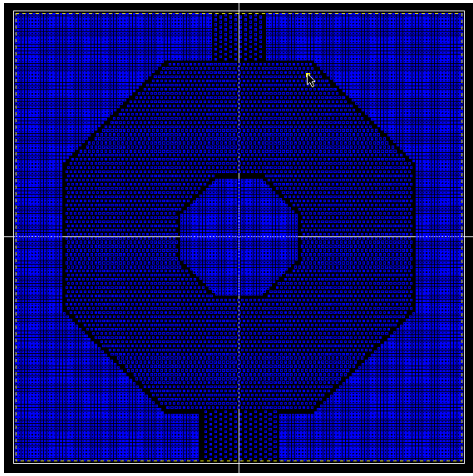
Top metal



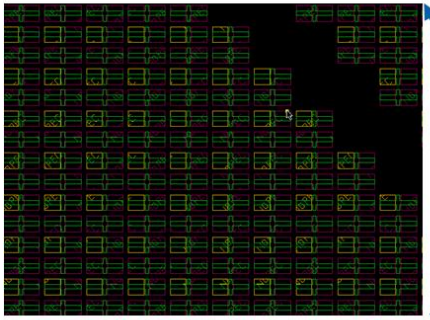
N-1



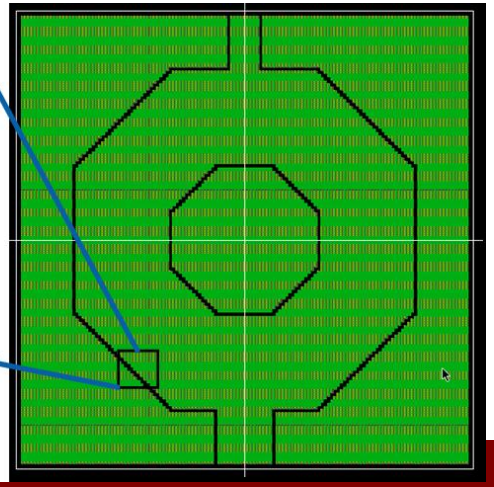
N-2

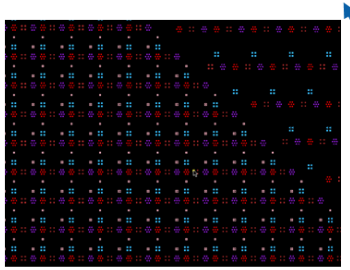


rest



Poly, diff





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