CATALYTE IC DESIGN

IC Design/ Methodology Training-Overview

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Dallas, TX

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Outline

- Services offered from CatalyteIC
- Course offerings for Q4_2010, Q1_2011
- Going forward- Q1-Q2, 2011
- Highlights- Sample Training modules
- FAQ
- How you can get involved
- Q/A

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Services offered from CatalyteIC

- www.catalyteic.com/ic-design/design-services
- www.catalyteic.com/training

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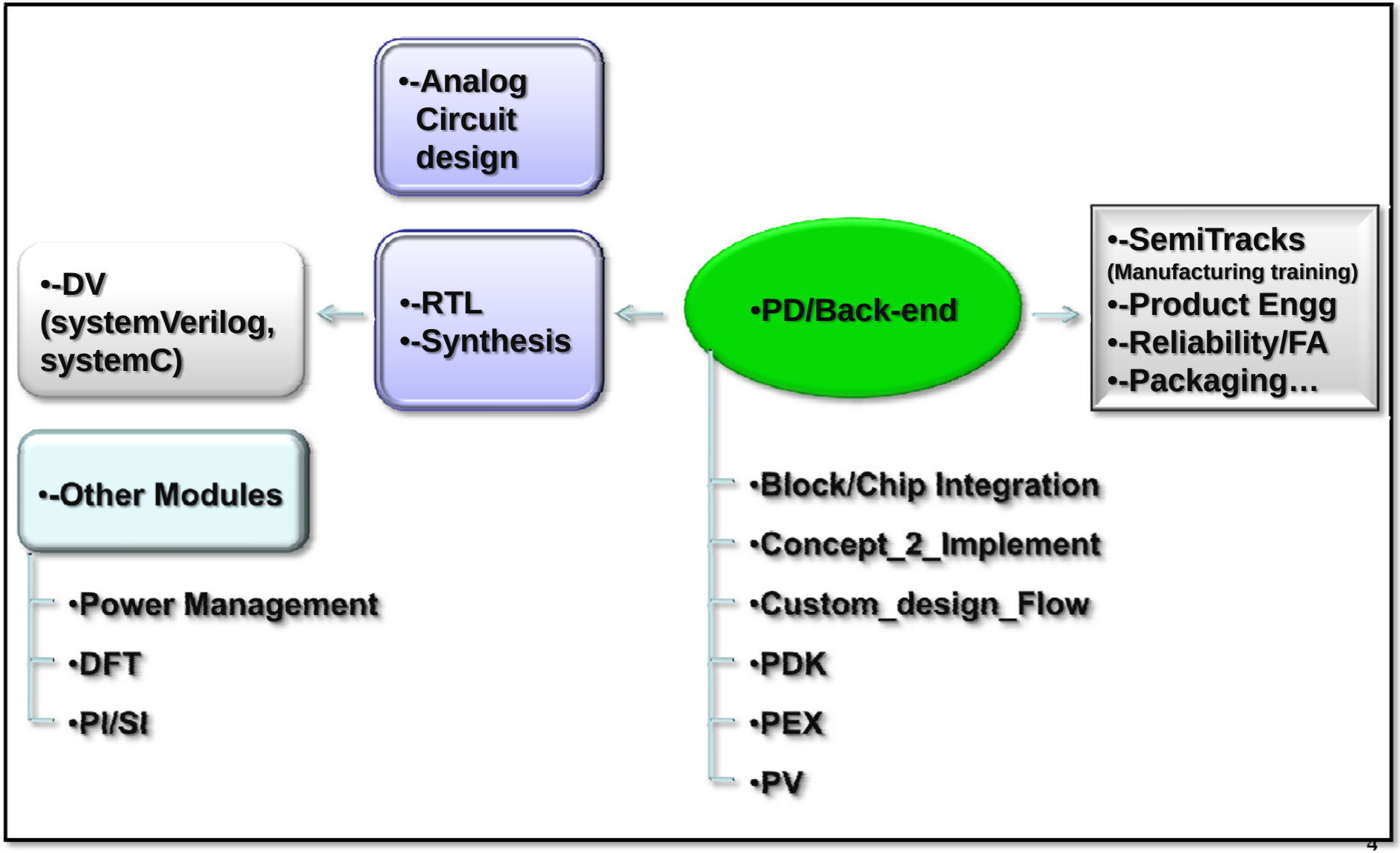
Extended services through collaboration



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The advantages of trainings from CatalyteIC

- Developers/Instructors- Industry experts with average 10-20 years of "real-world" experience in their areas of expertise.
- Modular course contents- addressing the needs of designers at all level.
- EDA tool and Technology independent. Emphasis on the "basic concepts" with simplified "real world" examples.
- Take the complete ownership of the problem. Training is just the first step toward a complete solution.
- Transforming yourself from a basic user to a power user.

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Course offerings for Q4_2010, Q1_2011

- http://www.catalyteic.com/ic-design/current-courses
- http://www.catalyteic.com/ic-design/upcoming-courses

- **Sample _1_page version of the training module-**

www.catalyteic.com/ic-design/soc-power-management-design-and-verification

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Near term event- Dec-Jan

- 30-45 min webinar on each module
- Another similar event in Jan_11

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Going forward- Q1-Q2, 2011

- Extending course offerings to major semiconductor cities (San Jose, Irvine, Boston, Portland, Phoenix…)
- 1-2 day workshops on entire set of CatalyteIC training modules (late Q1_11).

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Highlights- Sample Training module

- Custom Design Flow – Basic to Advanced- Faizul Alam
- SoC Power Management Design and Verification- Dr. Bhanu Kapoor
- Design and Verification with SystemC- Dr. Bhanu Kapoor
- Design and Productization of Digitally-Intensive RF Transceiver SoCs- Dr. Oren Eliezer
- Introduction to system verilog for designers and verification engineers- Paul Hylander

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FAQs

- **Course day**

Typically – 1 day long. Last 1-2 hr – Open session (real world problems) [9 to 5]

- **Refund Policy/ Discounts**

www.catalyteic.com/ic-design/catelyte-ic-design-cic-policy

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How you can get involved

- Spread the word
- Get engaged with CatalyteIC (In the _ES world- Be a module developer, Instructor, Take a course, Show where the pains are….)

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Q/A

Thank you

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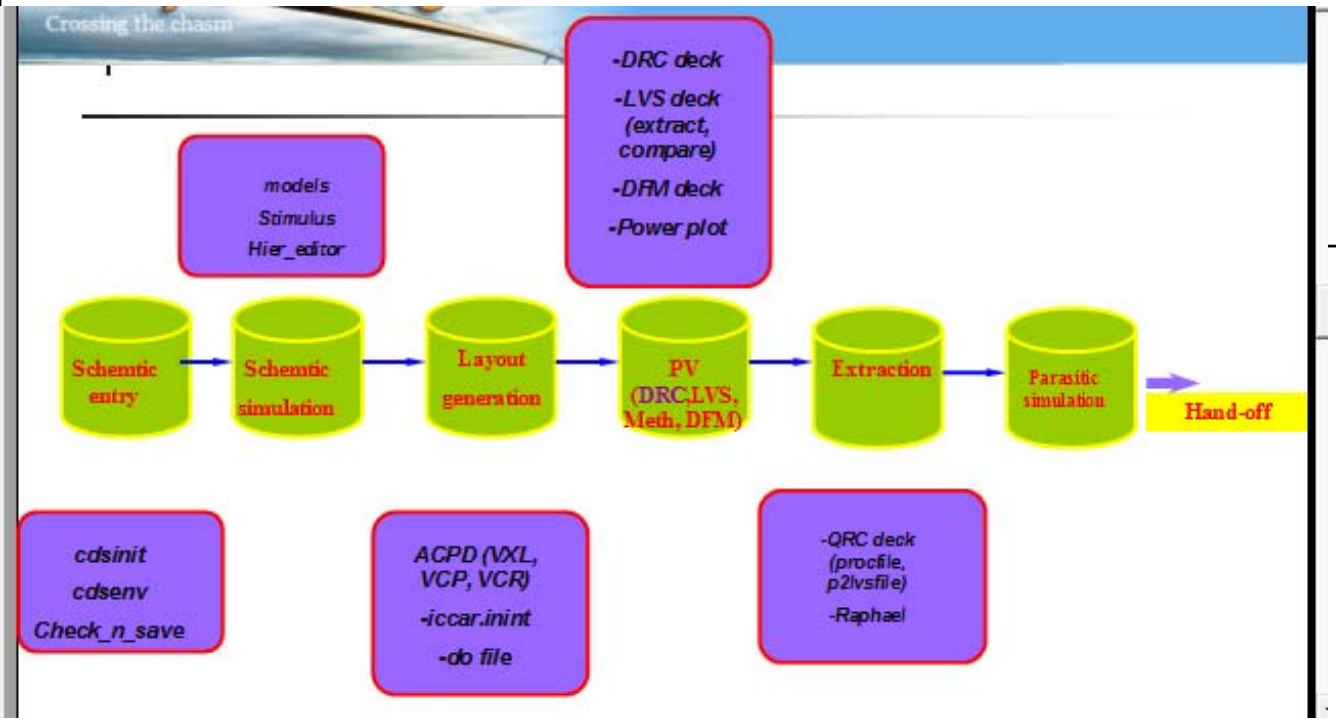
Backup slides

Custom Design Flow- Default To Power

Training Manual
July 15, 2009
Catalyte IC Design

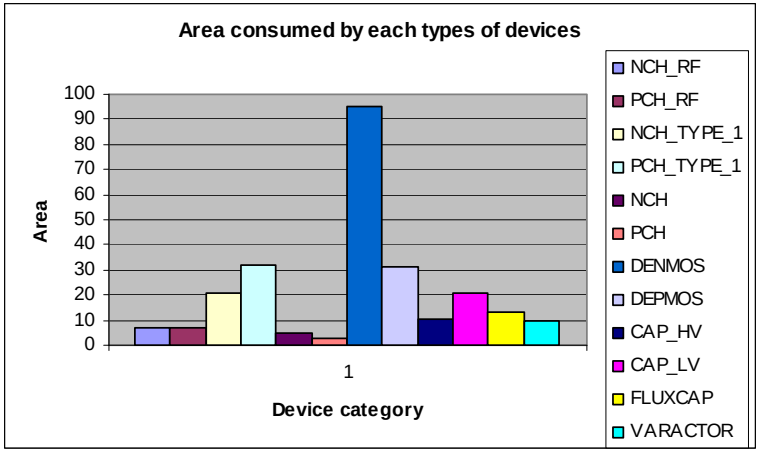


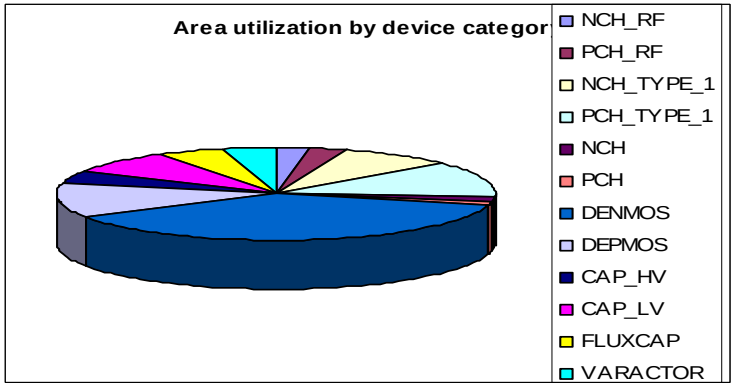
Advanced Topics

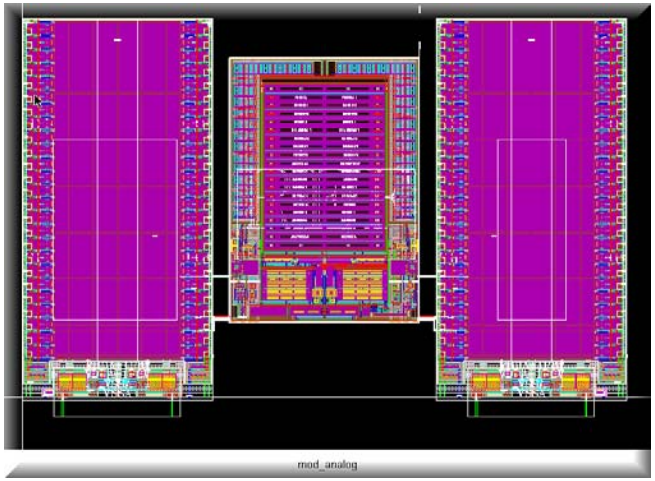
- ***Quantify Layout Utilization (QLU)***
- ***Parasitic Extraction Validation Flow***

- ***QRC Techfile generation- 6lm/7lm/8lm, min/nom/max, TC0/TC25.. (7d -> 1d -> 6 hr)***
- ***LVS deck (10k line -> 1k -> 50 line)***
- ***LVS deck (Options/ Switches)***
- ***Speed up DRC (deck split, design split, multi-CPU, LSF)***
- ***spice- 1_page_view***
- ***Parasitic extraction- 1_page_view***

QLU Illustration- Area used by various devices inside module mod_analog





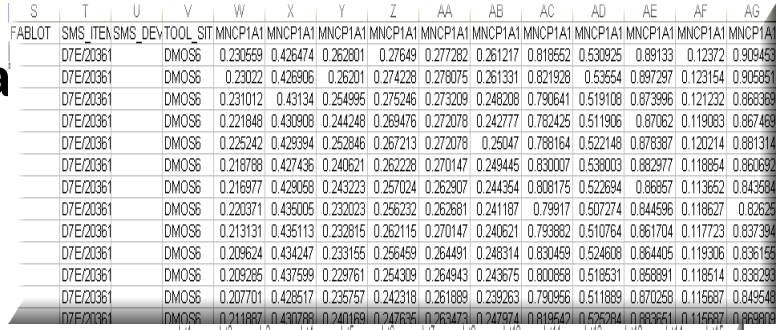


NCH_RF	6.6
PCH_RF	6.9
NCH_TYPI	20.6
PCH_TYPI	31.8
NCH	4.8
PCH	2.9
DENMOS	94.8
DEPMOS	31.4
CAP_HV	10.11
CAP_LV	20.6
FLUXCAP	12.9
VARACTO	9.7

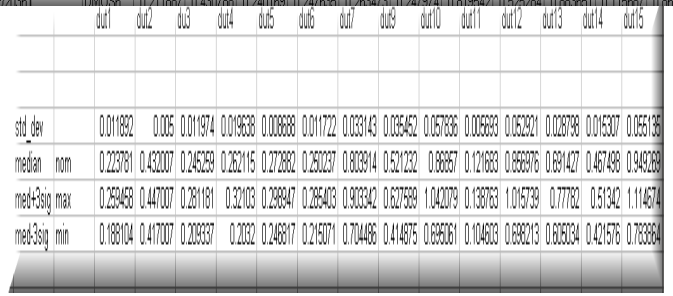
Area consumed by each device category

- Overall utilization of area by different categories of devices
- DENMOS consumed most spaces for mod_analog

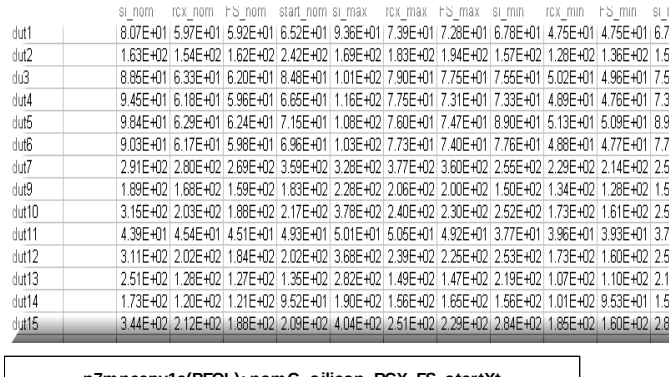
Parasitic Extraction Valida



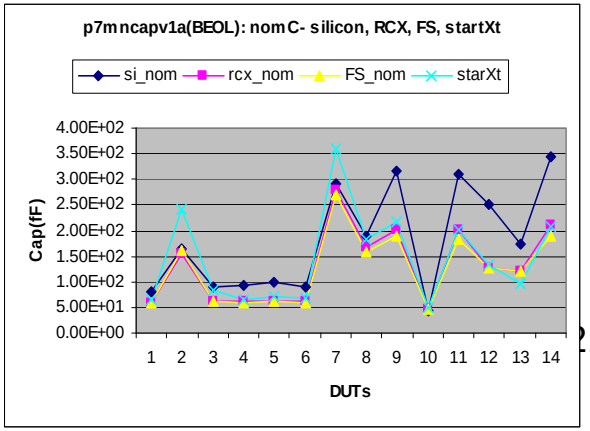
FABLOT	SMS_ITEM	SMS_DEV	TOOL_SIT	MNCP1A1	MNCP1A1	MNCP1A1	MNCP1A1	MNCP1A1	MNCP1A1	MNCP1A1	MNCP1A1	MNCP1A1	MNCP1A1	MNCP1A1
	D7E/20361		DMOS6	0.230559	0.426474	0.262801	0.27649	0.277282	0.261217	0.818552	0.530925	0.89133	0.12372	0.909453
	D7E/20361		DMOS6	0.23022	0.426906	0.26201	0.274228	0.278075	0.261331	0.821928	0.53554	0.897297	0.123154	0.905851
	D7E/20361		DMOS6	0.231012	0.43134	0.254995	0.275246	0.273209	0.248208	0.790641	0.519108	0.873996	0.121232	0.868369
	D7E/20361		DMOS6	0.221848	0.430908	0.244248	0.269476	0.272078	0.242777	0.782425	0.511906	0.87062	0.119083	0.867469
	D7E/20361		DMOS6	0.225242	0.429394	0.252846	0.267213	0.272078	0.25047	0.788164	0.522148	0.878387	0.120214	0.881314
	D7E/20361		DMOS6	0.219788	0.427436	0.240621	0.262228	0.270147	0.249445	0.830007	0.538003	0.882977	0.118854	0.860692
	D7E/20361		DMOS6	0.216977	0.429058	0.243223	0.257024	0.262907	0.244354	0.808175	0.522694	0.86857	0.113652	0.843584
	D7E/20361		DMOS6	0.220371	0.435005	0.232023	0.256232	0.262681	0.241187	0.79917	0.507274	0.844596	0.118627	0.82625
	D7E/20361		DMOS6	0.213131	0.435113	0.232815	0.262115	0.270147	0.240621	0.793862	0.510764	0.861704	0.117723	0.837394
	D7E/20361		DMOS6	0.209624	0.434247	0.233155	0.256459	0.264491	0.248314	0.830459	0.524608	0.864405	0.119306	0.836155
	D7E/20361		DMOS6	0.209285	0.437599	0.229761	0.254309	0.264943	0.243675	0.800858	0.518531	0.858891	0.118514	0.838293
	D7E/20361		DMOS6	0.207701	0.428517	0.235757	0.242318	0.261888	0.239263	0.790956	0.511889	0.870258	0.115687	0.849548
	D7E/20361		DMOS6	0.211887	0.430788	0.240169	0.247635	0.263473	0.247974	0.819542	0.525284	0.883651	0.116687	0.869806

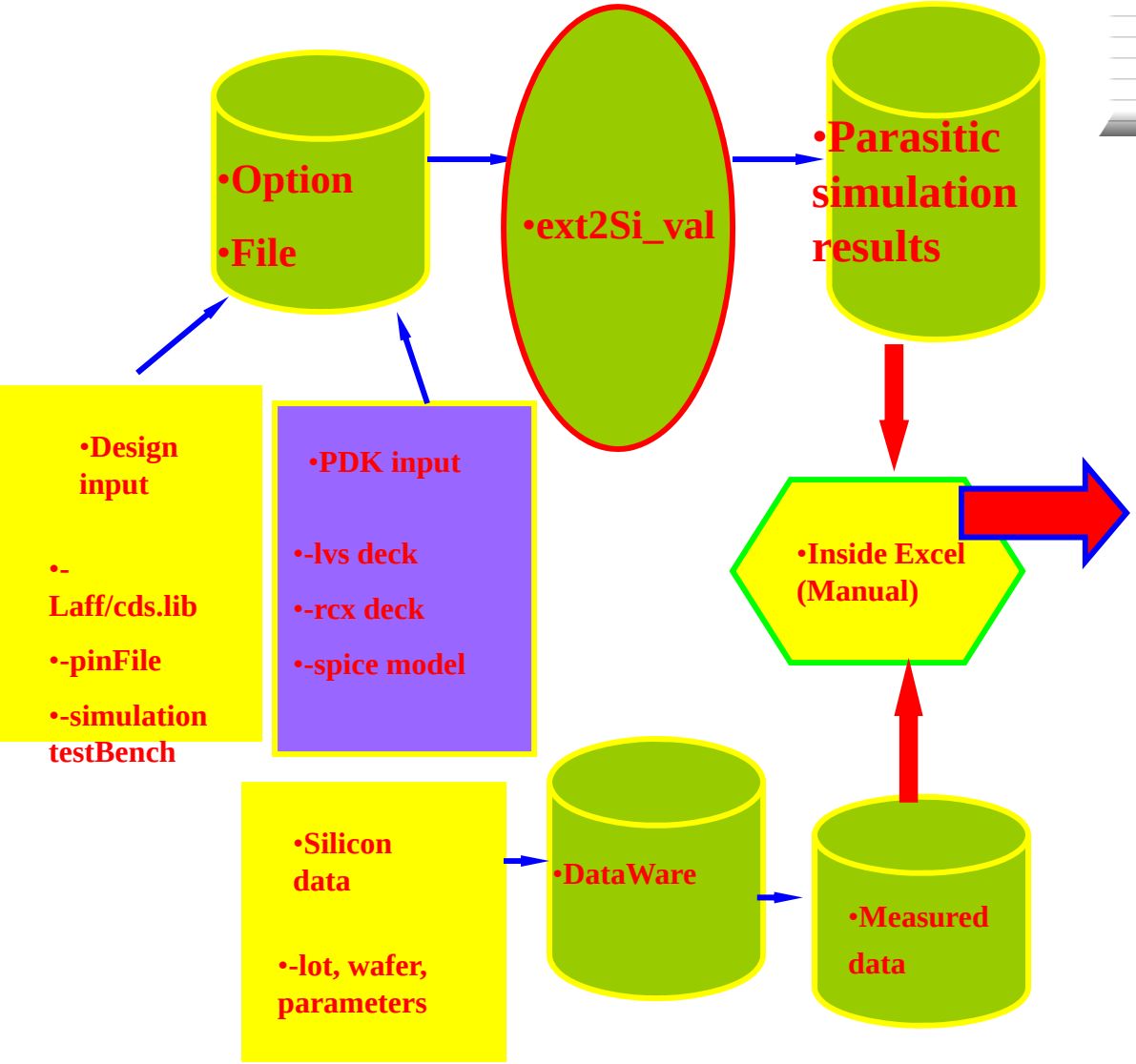


		dut1	dut2	dut3	dut4	dut5	dut6	dut7	dut8	dut10	dut11	dut12	dut13	dut14	dut15
std_dev		0.011892	0.005	0.011974	0.019638	0.006688	0.011722	0.033143	0.035452	0.057636	0.005693	0.052921	0.028798	0.015307	0.055136
median	nom	0.223781	0.432007	0.245259	0.262115	0.272862	0.250237	0.803914	0.521232	0.86857	0.121683	0.866976	0.691427	0.467498	0.949268
med+3sig	max	0.259458	0.447007	0.281181	0.32103	0.293947	0.265403	0.903342	0.627589	1.042079	0.138763	1.015739	0.77782	0.51342	1.114674
med-3sig	min	0.188104	0.417007	0.208337	0.2032	0.246817	0.215071	0.704486	0.414875	0.695061	0.104603	0.716213	0.605034	0.421576	0.783664

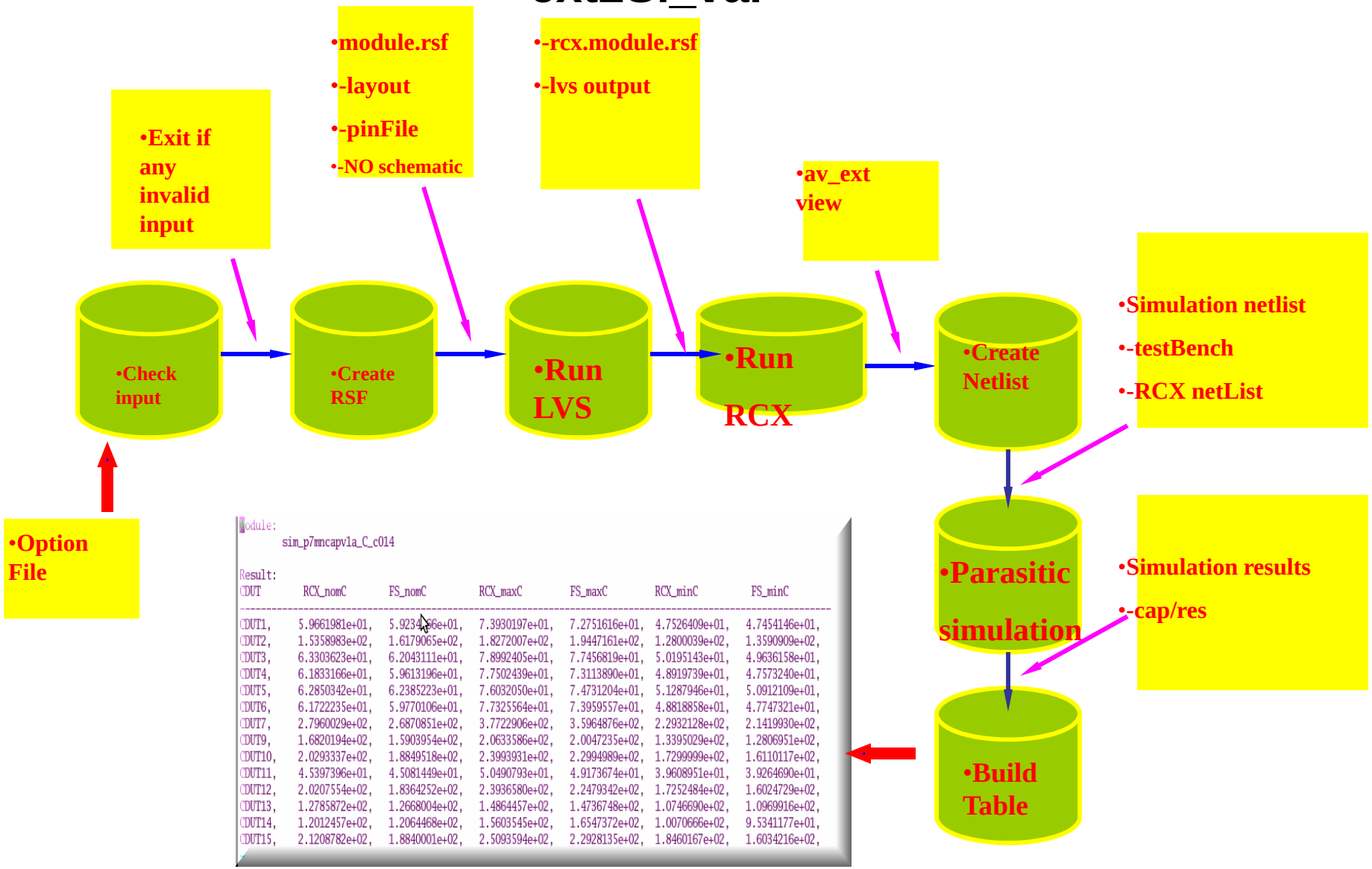


	si_nom	rcx_nom	FS_nom	start_nom	si_max	rcx_max	FS_max	si_min	rcx_min	FS_min	si_
dut1	8.07E+01	5.97E+01	5.92E+01	6.52E+01	9.36E+01	7.39E+01	7.28E+01	6.78E+01	4.75E+01	4.75E+01	6.7
dut2	1.63E+02	1.54E+02	1.62E+02	2.42E+02	1.69E+02	1.83E+02	1.94E+02	1.57E+02	1.28E+02	1.36E+02	1.5
dut3	8.85E+01	6.33E+01	6.20E+01	8.48E+01	1.01E+02	7.90E+01	7.75E+01	7.55E+01	5.02E+01	4.96E+01	7.5
dut4	9.45E+01	6.18E+01	5.96E+01	6.65E+01	1.16E+02	7.75E+01	7.31E+01	7.33E+01	4.89E+01	4.76E+01	7.3
dut5	9.84E+01	6.29E+01	6.24E+01	7.15E+01	1.08E+02	7.60E+01	7.47E+01	8.90E+01	5.13E+01	5.09E+01	8.9
dut6	9.03E+01	6.17E+01	5.98E+01	6.96E+01	1.03E+02	7.73E+01	7.40E+01	7.76E+01	4.88E+01	4.77E+01	7.7
dut7	2.91E+02	2.80E+02	2.69E+02	3.59E+02	3.28E+02	3.77E+02	3.60E+02	2.55E+02	2.29E+02	2.14E+02	2.5
dut9	1.89E+02	1.68E+02	1.59E+02	1.83E+02	2.28E+02	2.06E+02	2.00E+02	1.50E+02	1.34E+02	1.28E+02	1.5
dut10	3.15E+02	2.03E+02	1.88E+02	2.17E+02	3.78E+02	2.40E+02	2.30E+02	2.52E+02	1.73E+02	1.61E+02	2.5
dut11	4.39E+01	4.54E+01	4.51E+01	4.93E+01	5.01E+01	5.05E+01	4.92E+01	3.77E+01	3.96E+01	3.93E+01	3.7
dut12	3.11E+02	2.02E+02	1.84E+02	2.02E+02	3.68E+02	2.39E+02	2.25E+02	2.53E+02	1.73E+02	1.60E+02	2.5
dut13	2.51E+02	1.28E+02	1.27E+02	1.35E+02	2.82E+02	1.49E+02	1.47E+02	2.19E+02	1.07E+02	1.10E+02	2.1
dut14	1.73E+02	1.20E+02	1.21E+02	9.52E+01	1.90E+02	1.56E+02	1.65E+02	1.56E+02	1.01E+02	9.53E+01	1.5
dut15	3.44E+02	2.12E+02	1.88E+02	2.09E+02	4.04E+02	2.51E+02	2.29E+02	2.84E+02	1.85E+02	1.60E+02	2.8





ext2Si_val



odule:
sim_p7mncapv1a_C_c014

Result:

CDUT	RCX_nomC	FS_nomC	RCX_maxC	FS_maxC	RCX_minC	FS_minC
CDUT1,	5.9661981e+01,	5.9234166e+01,	7.3930197e+01,	7.2751616e+01,	4.7526409e+01,	4.7454146e+01,
CDUT2,	1.5358983e+02,	1.6179065e+02,	1.8272007e+02,	1.9447161e+02,	1.2800039e+02,	1.3590909e+02,
CDUT3,	6.3303623e+01,	6.2043111e+01,	7.8992405e+01,	7.7456819e+01,	5.0195143e+01,	4.9636158e+01,
CDUT4,	6.1833166e+01,	5.9613196e+01,	7.7502439e+01,	7.3113890e+01,	4.8919739e+01,	4.7573240e+01,
CDUT5,	6.2850342e+01,	6.2385223e+01,	7.6032050e+01,	7.4731204e+01,	5.1287946e+01,	5.0912109e+01,
CDUT6,	6.1722235e+01,	5.9770106e+01,	7.7325564e+01,	7.3959557e+01,	4.8818858e+01,	4.7747321e+01,
CDUT7,	2.7960029e+02,	2.6870851e+02,	3.7722906e+02,	3.5964876e+02,	2.2932128e+02,	2.1419930e+02,
CDUT9,	1.6820194e+02,	1.5903954e+02,	2.0633586e+02,	2.0047235e+02,	1.3395029e+02,	1.2806951e+02,
CDUT10,	2.0293337e+02,	1.8849518e+02,	2.3993931e+02,	2.2994989e+02,	1.7299999e+02,	1.6110117e+02,
CDUT11,	4.5397396e+01,	4.5081449e+01,	5.0490793e+01,	4.9173674e+01,	3.9608951e+01,	3.9264690e+01,
CDUT12,	2.0207554e+02,	1.8364252e+02,	2.3936580e+02,	2.2479342e+02,	1.7252484e+02,	1.6024729e+02,
CDUT13,	1.2785872e+02,	1.2668004e+02,	1.4864457e+02,	1.4736748e+02,	1.0746690e+02,	1.0969916e+02,
CDUT14,	1.2012457e+02,	1.2064468e+02,	1.5603545e+02,	1.6547372e+02,	1.0070666e+02,	9.5341177e+01,
CDUT15,	2.1208782e+02,	1.8840001e+02,	2.5093594e+02,	2.2928135e+02,	1.8460167e+02,	1.6034216e+02,

•EDA Tools/Terminology- Simplified

Function	Cadence	Synopsys	Mentor	Magma	IDM1	IDM2	Comments
Schematic	Composer	Galaxy	-	-	-	-	-
Circuit simulation	spectre	Hspice	-	-	Power spice	Spectre	-
Fast Spice	ultra-sim	Nano-sim	-	finesim	-	-	-
Layout (Manual)	VLE	Galaxy	IC-Station	-	-	-	-
Automated system layout	VXL,VCP VCR	Orion	-	-	-	-	Laker
Physical Verification -DRC -LVS -ERC	Assura (PVS, Dracula, Diva, Vampire)	Hercules	Calibre	Quartz DRC/LVS	Niagara	Hercules K2 (GV,SV)	-
Parasitic Extraction (R, C, L, K)	QRC (RCX)	Star-RCXT	Xcalibre	Quartz RC	Erie	QRC Star-RCXT	-Raphael, QuickCap
Database							
Tapeout	-	-	-	-	RIT	PG	
Layout DB	DFII/OA	Milkyway	-	Volcano			
DFM	LPA LEA	LCC CMP	-LFD yieldEnhancer	Yield-Analyzer	-	-	-